

Compal Confidential

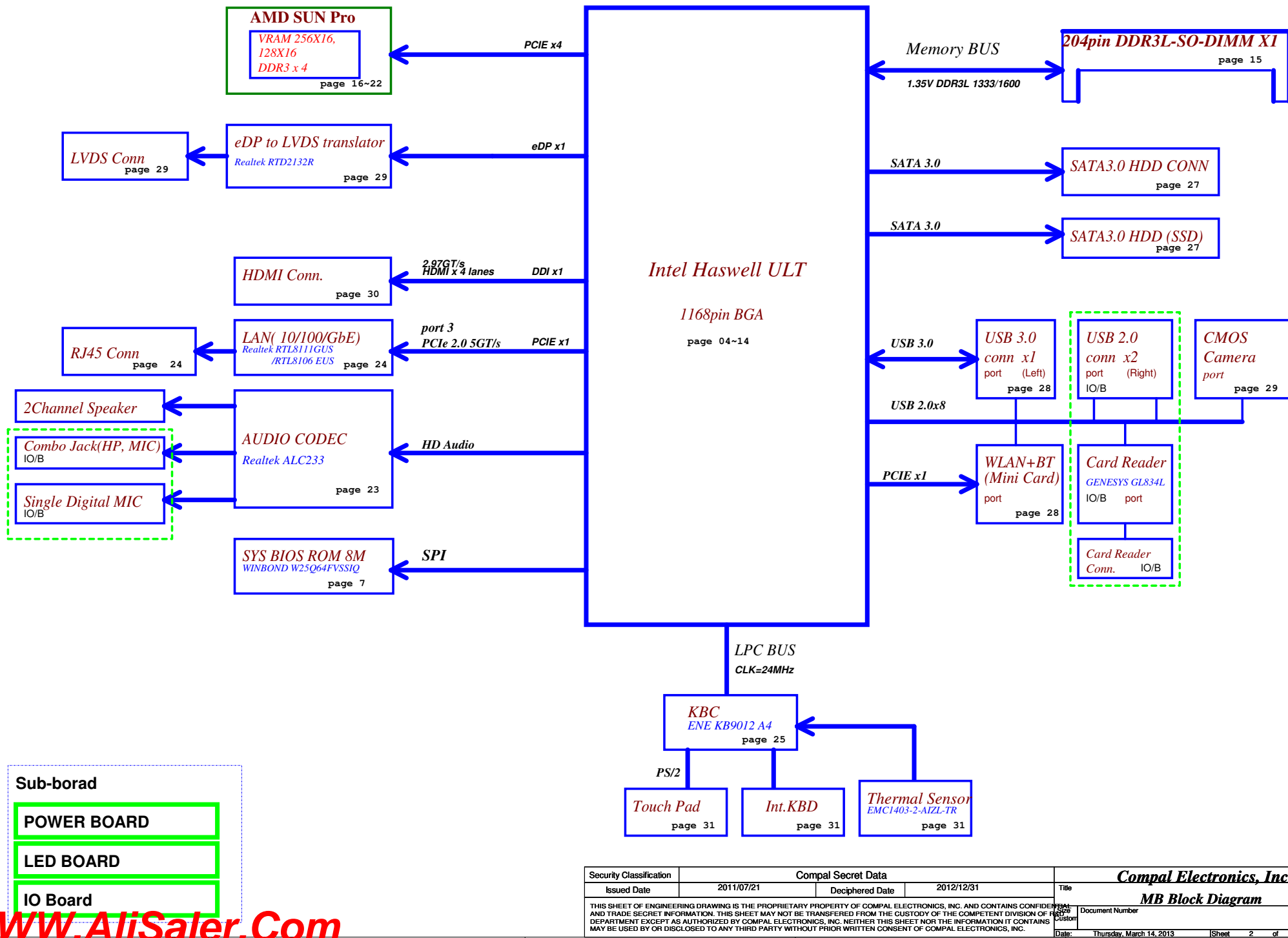
Model Name : ZIUS6/S7
File Name : LA-A321PR01
BOM P/N:4319OP38L5x -- ZIUS7
4319OP38L0x -- ZIUS6

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ZIUS6/S7 M/B Schematics Document
Intel SharyBay ULT Processor + AMD SUN Pro

2013-03-14
REV: 0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title Cover Page
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Voltage Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS +VGA_CORE (PX) +0.95VS_VGA (PX) +3.3VS_VGA (PX) +1.8VS_VGA (PX) +1.5VS_VGA (PX)
State		+3VALW		
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	0.1
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
CPU OPTION	CPU1@
INTEL UMA	UMA@
AMD SUN Pro	PX@
VRAM Option	S1G@ M1G@ H1G@ S2G@ M2G@
LAN RTL8111GUS	8111@ SWR@
LAN RTL8106EUS	8106@ SWR@
USB3.0	USB3@
EMI PART	EMI@
ESD PART	ESD@

EC SM Bus1 address

Device	Address
Smart Battery Charger	

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AI2L-TR Panel - eDP to LVDS translator SharkBay ULT AMD SUN Pro	1001_101xb

CPU SM Bus address

Device	Address
DDR DIMM0 WALN Touch Pad	0XA0

CPU SML0 Bus address

Device	Address
--------	---------

USB 2.0 Port Table

Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	USB 2.0 Port (I/O Board)
3	Card Reader
4	Touch Screen (reserve)
5	Camera
6	Mini Card (WLAN/BT)
7	

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

PCIe Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		
5	0	
	1	
	2	GPU
	3	
6	0	
	1	
	2	
	3	

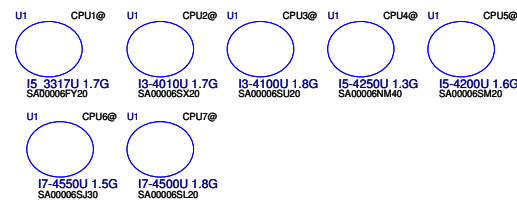
SATA Port Table

Port	
3	
2	
1	mSATA SSD
0	HDD

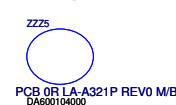
SMBUS Control Table

	HOST	VGA	BATT	KB9012	SODIMM	WLAN	PANEL sensor ADM1032	Thermal sensor EMC1403	VGA sensor ADM1032	CPU Sensor	Touch Pad	Security ROM	NFC
EC_SMB_CK1 EC_SMB_DA1	KB9012 +3VLP	X	+3VLP	X	X	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9012 +3VS	+3VS	X	X	X	X	+3VS	+3VS	+3VS	+3VALW	X	X	X
SMBCLK SMBDATA	CPU +3VALW	X	X	X	+3VS	+3VS	X	X	X	X	+3VS	+3VS	+3VS
SMLCLK SML0DATA	CPU +3VALW	X	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	KB9012 +3VS	X	X	+3VS	X	X	X	X	X	+3VALW	X	X	X

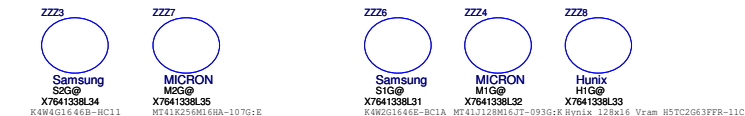
CPU part



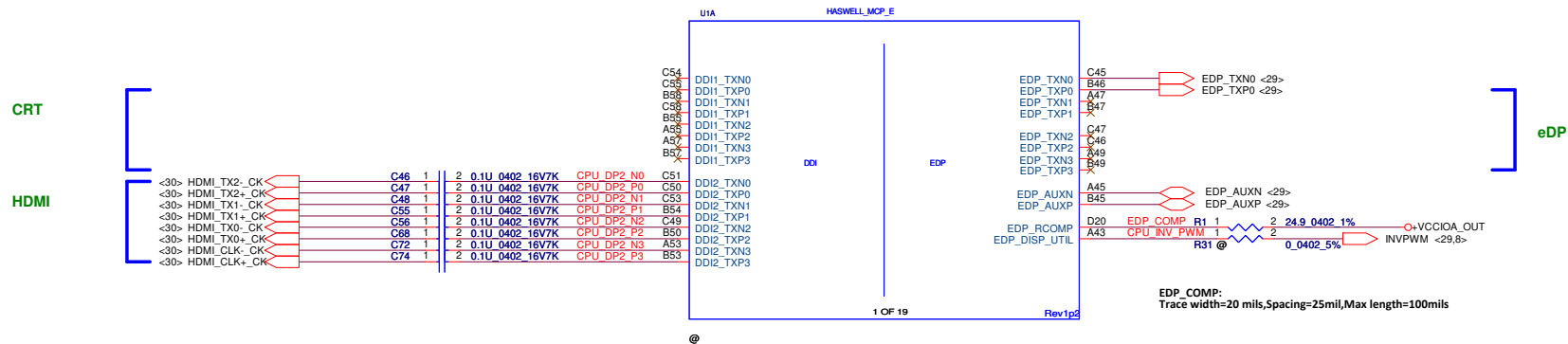
PCB part



VRAM

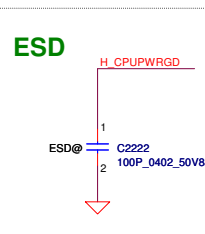
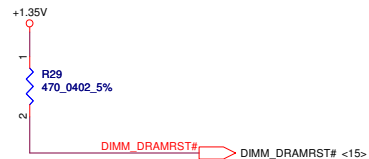


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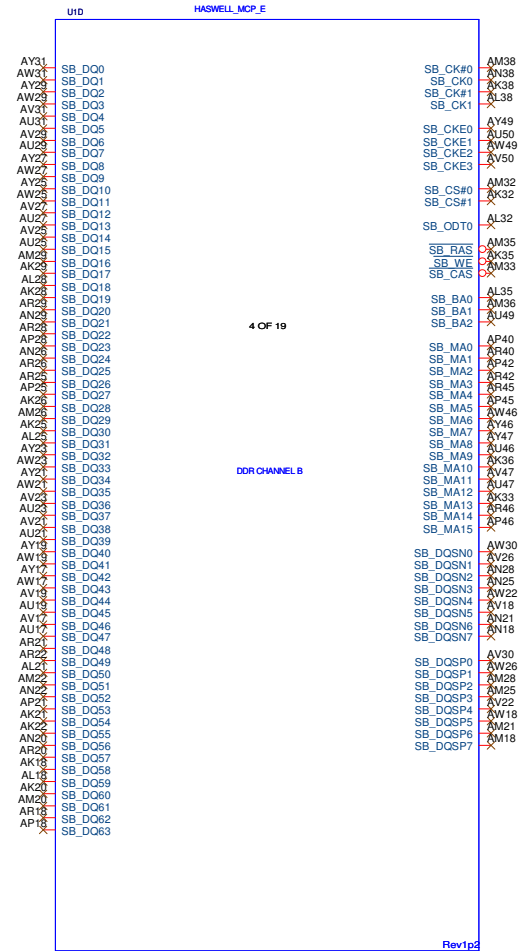
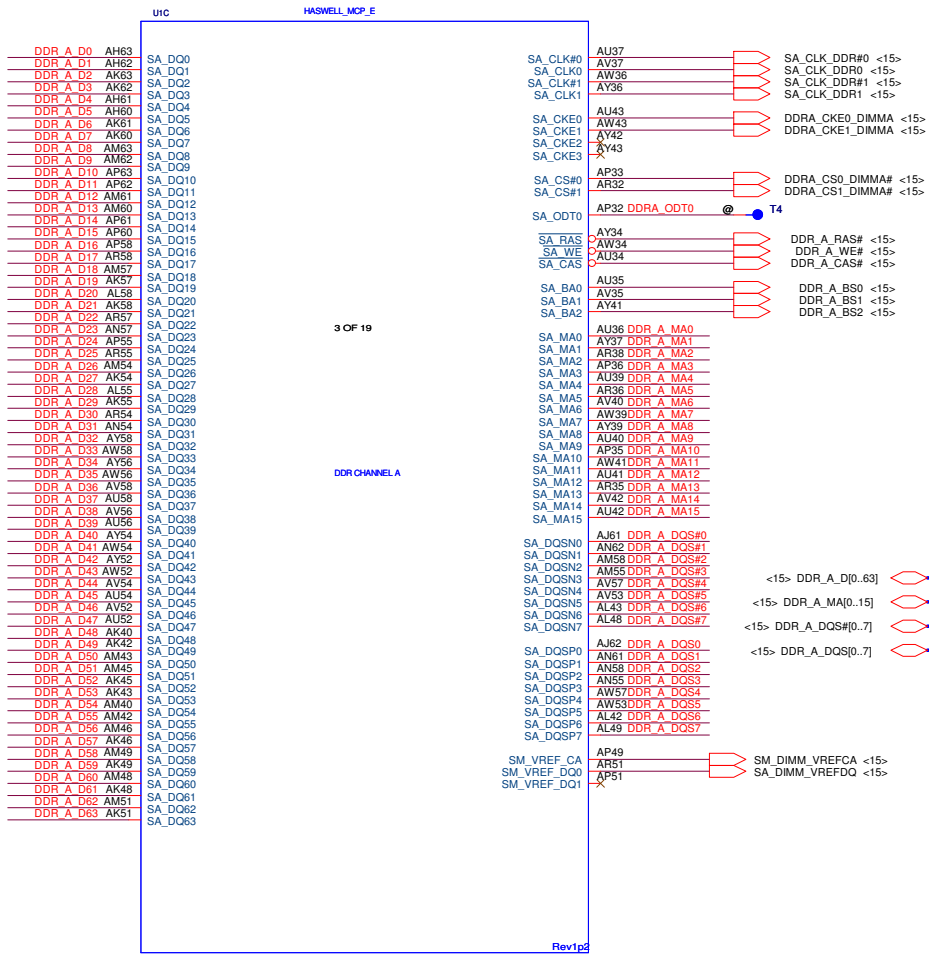


DDR3 Compensation Signals:
 20mils to comp signals
 25mils to non-comp signals
 500mil for Max trace length

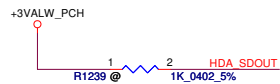
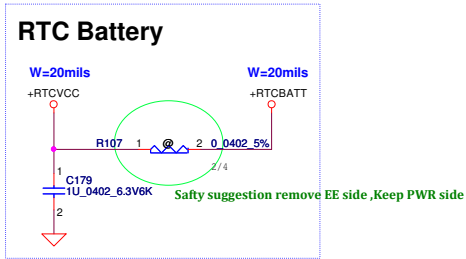
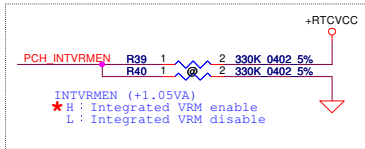
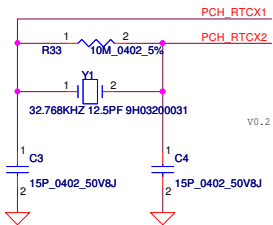
Chklist 1.0
 SM_RCOMP1 -->120 ohm 1%



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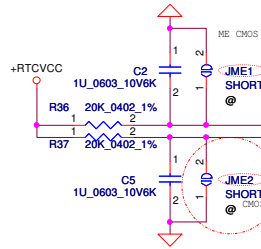


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						Date					

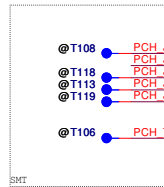


HDA_SDOUT
 ME debug mode, this signal has a weak internal PD
 * Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]

JME2 Short PAD placement to Bottom side.



<23> HDA_SDIN0



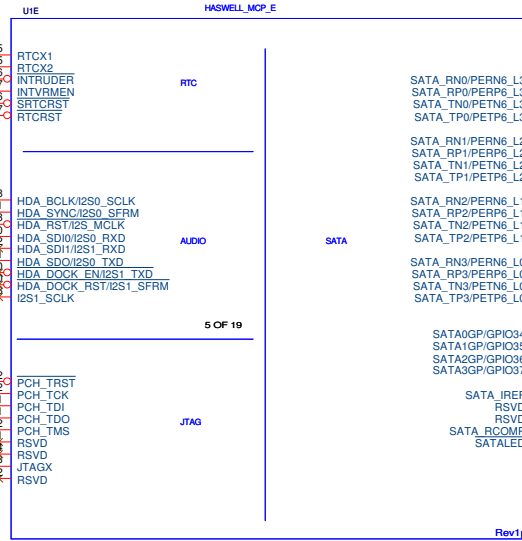
EMI

<23> HDA_SDOUT_AUDIO
 <23> HDA_SYNC_AUDIO
 <23> HDA_RST_AUDIO#
 <23> HDA_BITCLK_AUDIO

RF

C5205 @
 68P_0402_50V6J

<25> ME_FLASH



HDD
 mSATA

+1.05VS_ASATA3PLL
 EC_SMI#
 PCH_GPIO35
 PCH_GPIO36
 PCH_GPIO37

SATA_RCOMP
 PCH_SATALED#
 PCH_SATALED#

+3VS
 R99 1 2 10K 0402_5% EC_SMI#

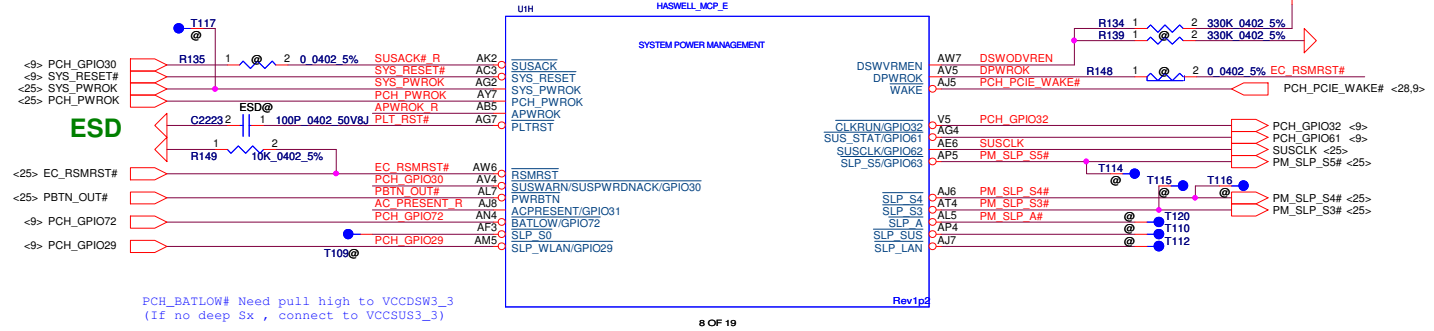
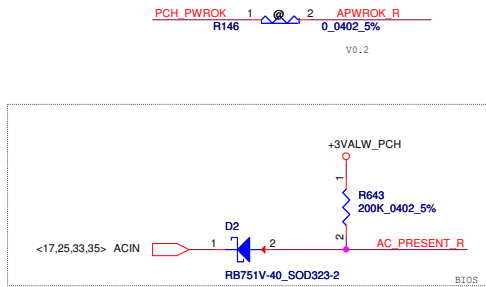
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2012/12/13				Title				HWS MCP(3/11) RTC,SATA,XDP			
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Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit

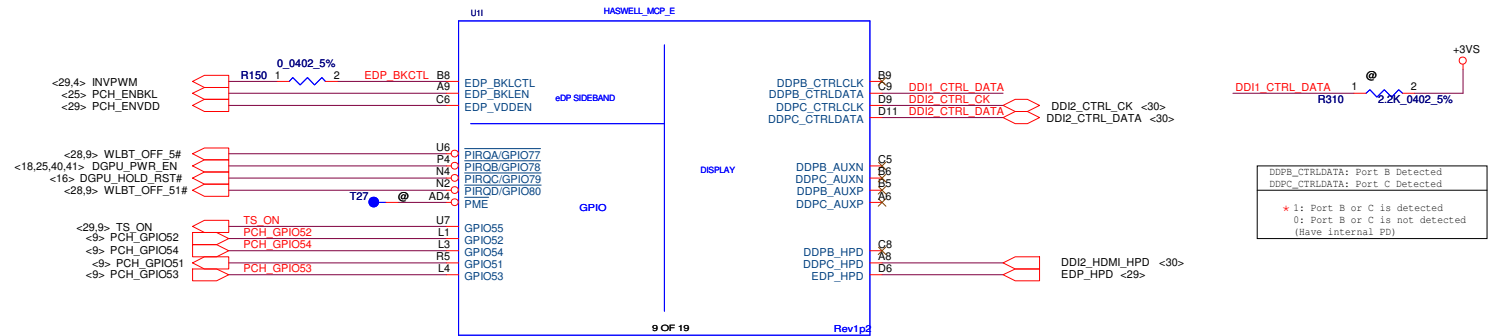
CAN be NC ,if not support Deep Sx

DPWROK: Tied together with RSMRST# that do not support Deep Sx

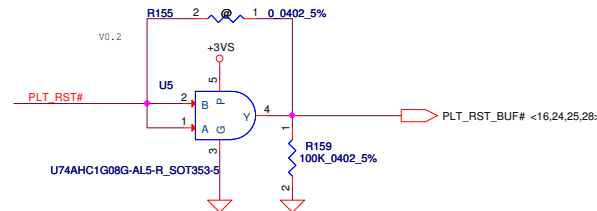
DSWODVREN - On Die DSW VR Enable
★ H : Enable (DEFAULT)
L : Disable



PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx , connect to VCCSUS3_3)



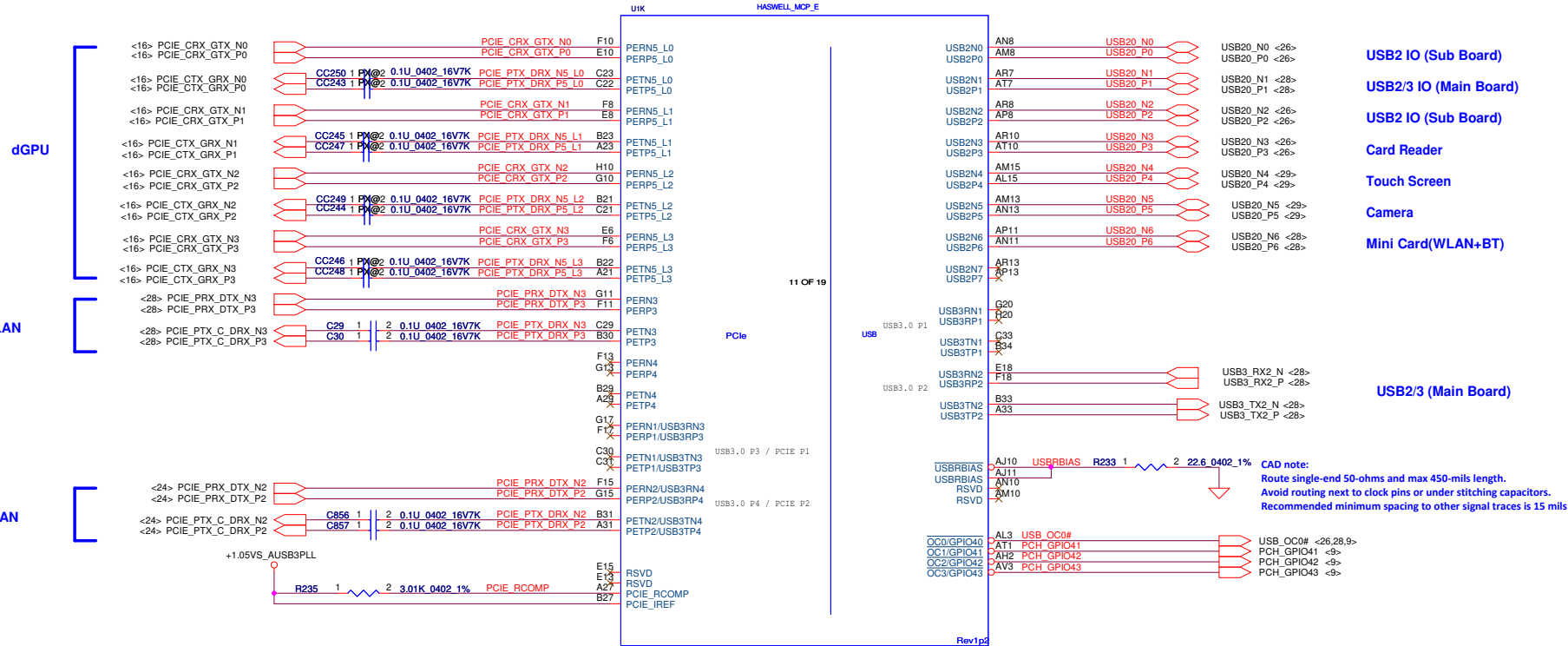
DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected
★ 1: Port B or C is detected
0: Port B or C is not detected (Have internal PD)



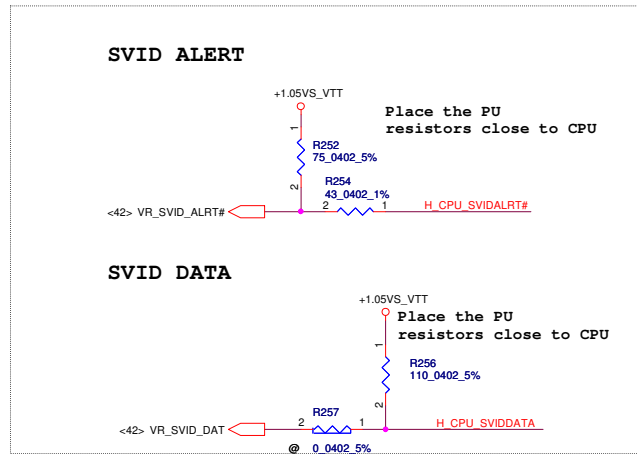
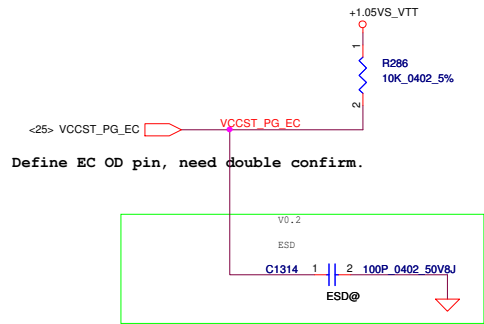
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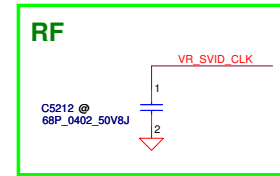
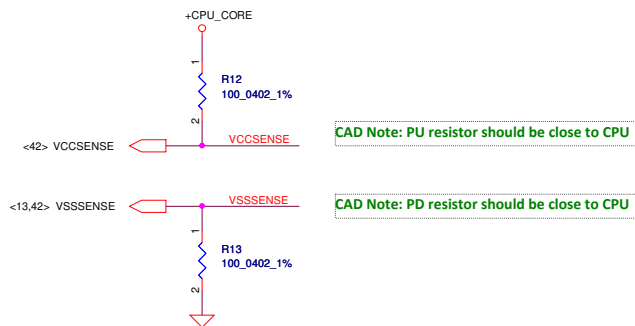
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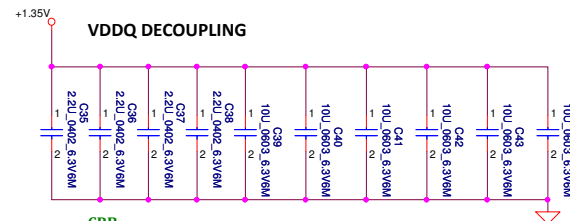
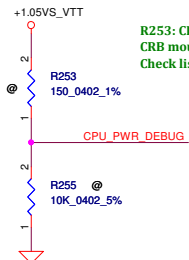
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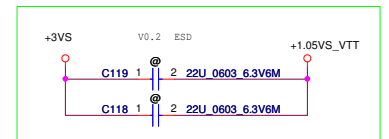
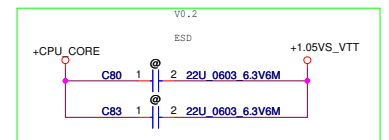
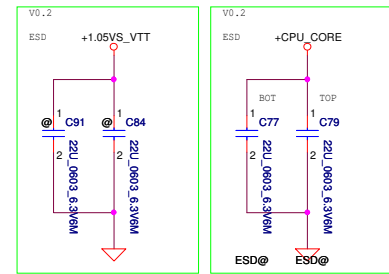
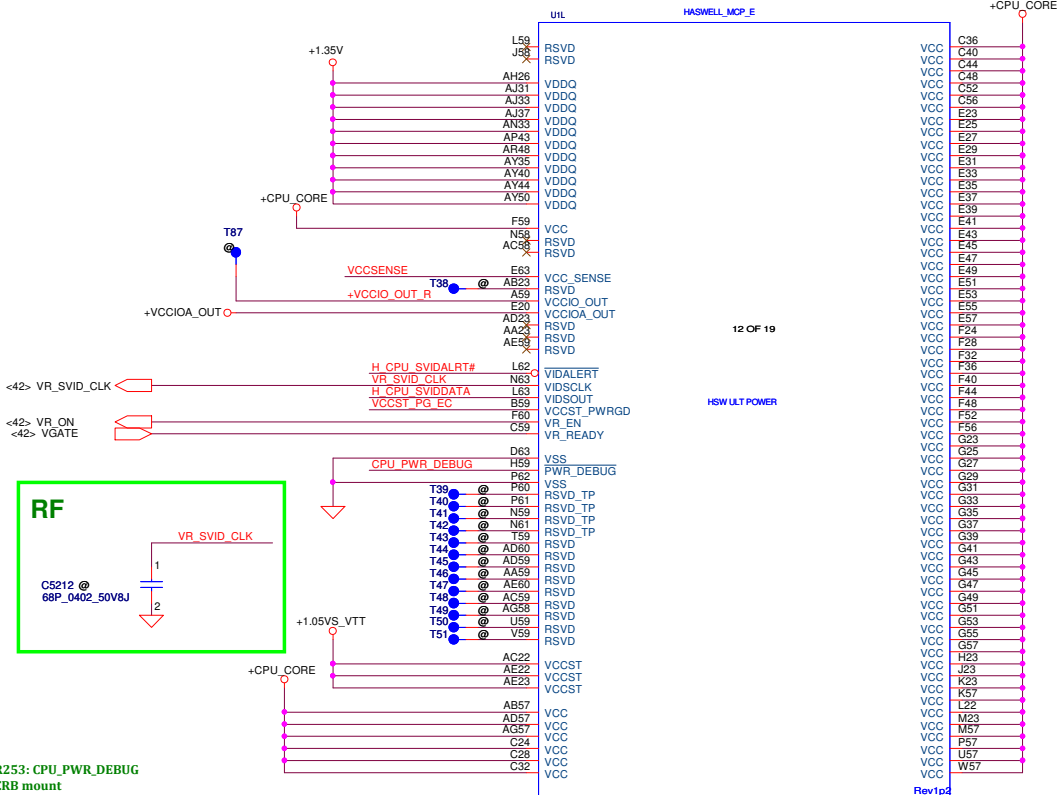
R256:
CRB r0.7 changed from 130 Ohms to 110 Ohms



R253: CPU_PWR_DEBUG
CRB mount
Check list_XDP use only

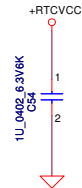
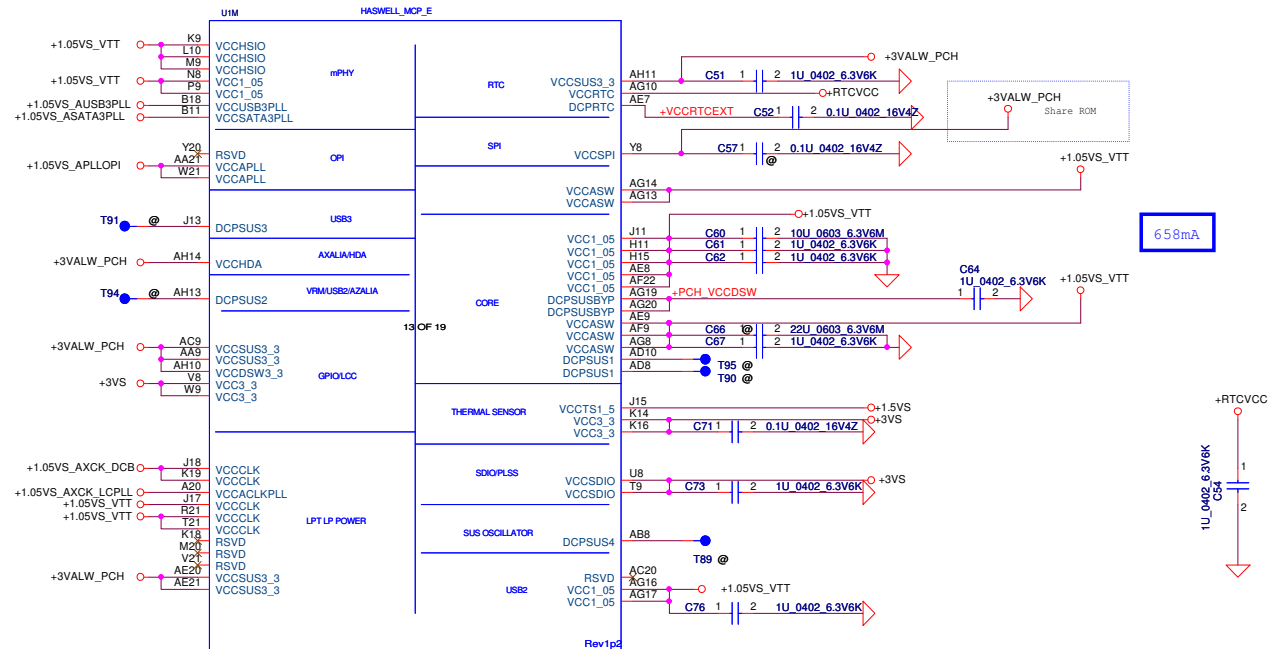
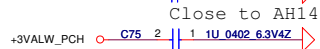
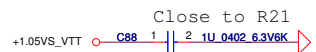
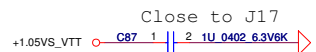
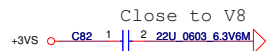
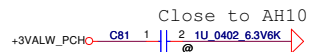
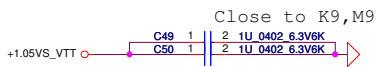
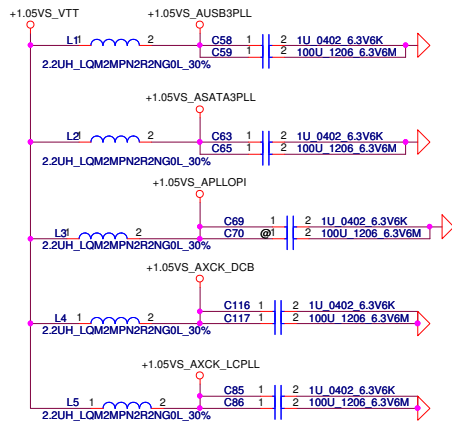


CRB:
+1.35V : 470UF/2V/7343 *2 (Un-mount)
10UF/6.3V/0603 *6
2.2UF/6.3V/0402 *4

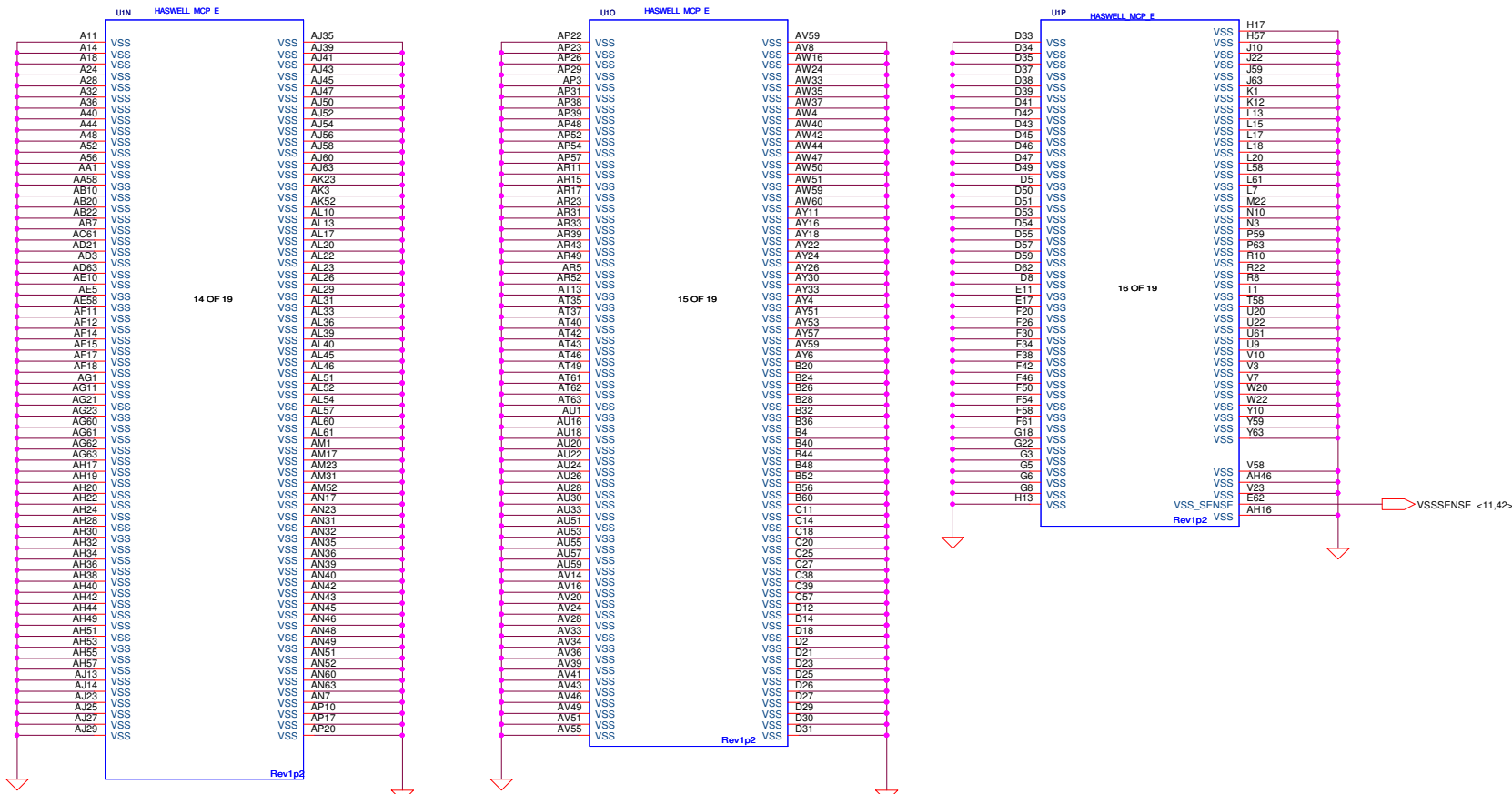


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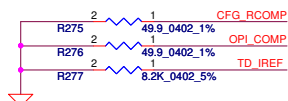
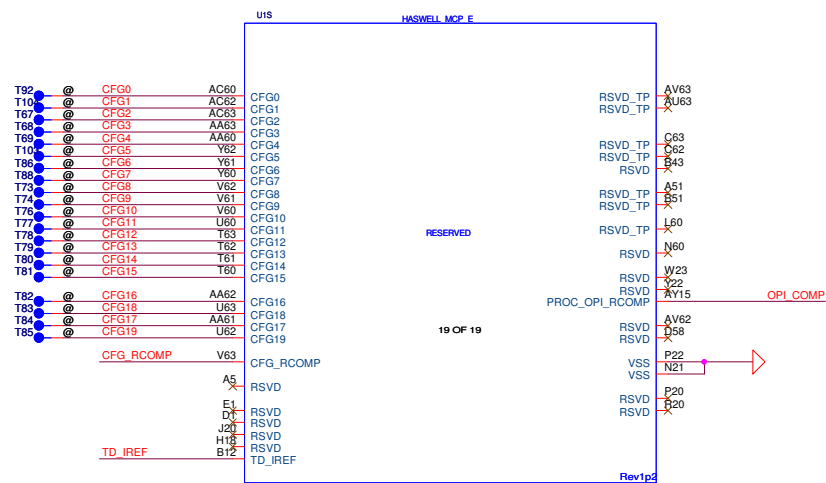
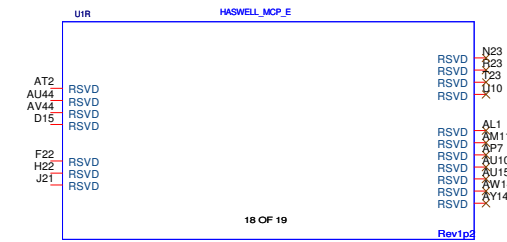
Check Power Source Close to N8
+1.05VS_VTT C53 @ 2 1U 0402 6.3V6K



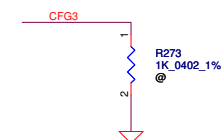
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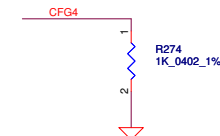
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				Document Number		Rev	
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				Date: Thursday, March 14, 2013		Sheet 13 of 46	



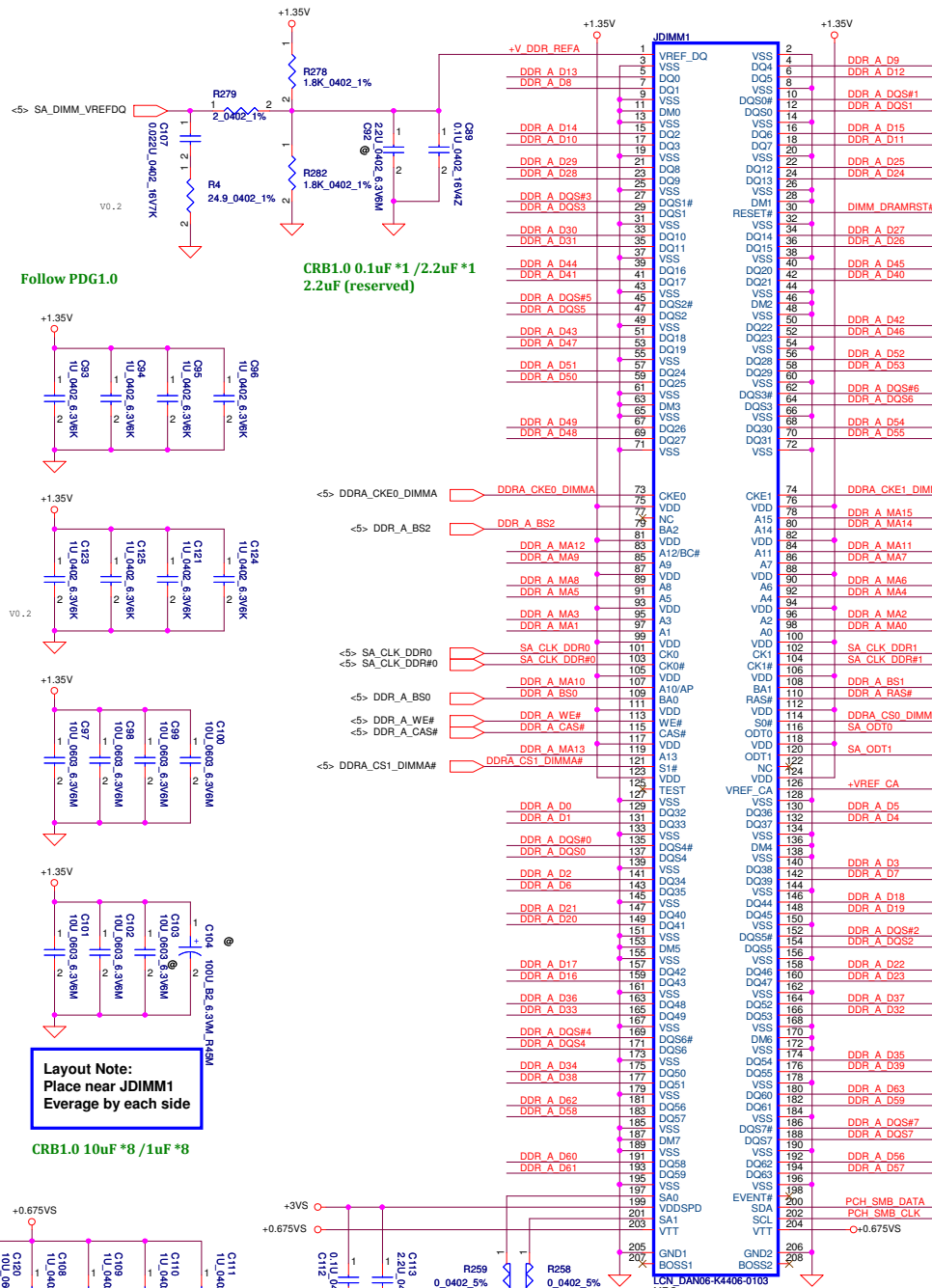
CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



All VREF traces should have 10 mil trace width

Follow PDG1.0

CRB1.0 0.1uF *1 / 2.2uF *1
2.2uF (reserved)

Layout Note:
Place near JDIMM1
Everage by each side

CRB1.0 10uF *8 / 1uF *8

Layout Note:
Place near JDIMM1.203,204

CRB1.0 0.1uF *1 / 1uF *1

CHANNEL A /TYPE :Reverse / H:4mm

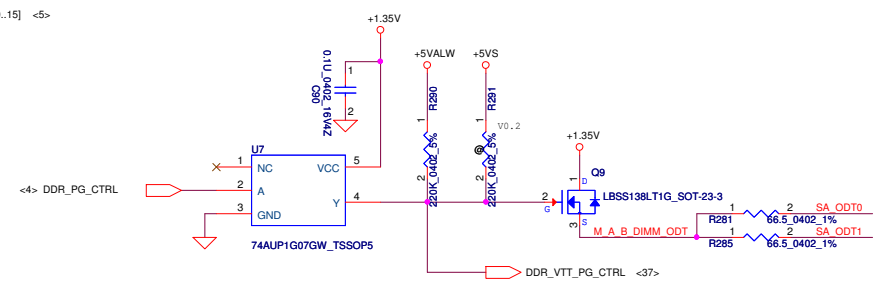
CHA SPD ADDRESS IS 0xA0

CHA TS ADDRESS IS 0x30

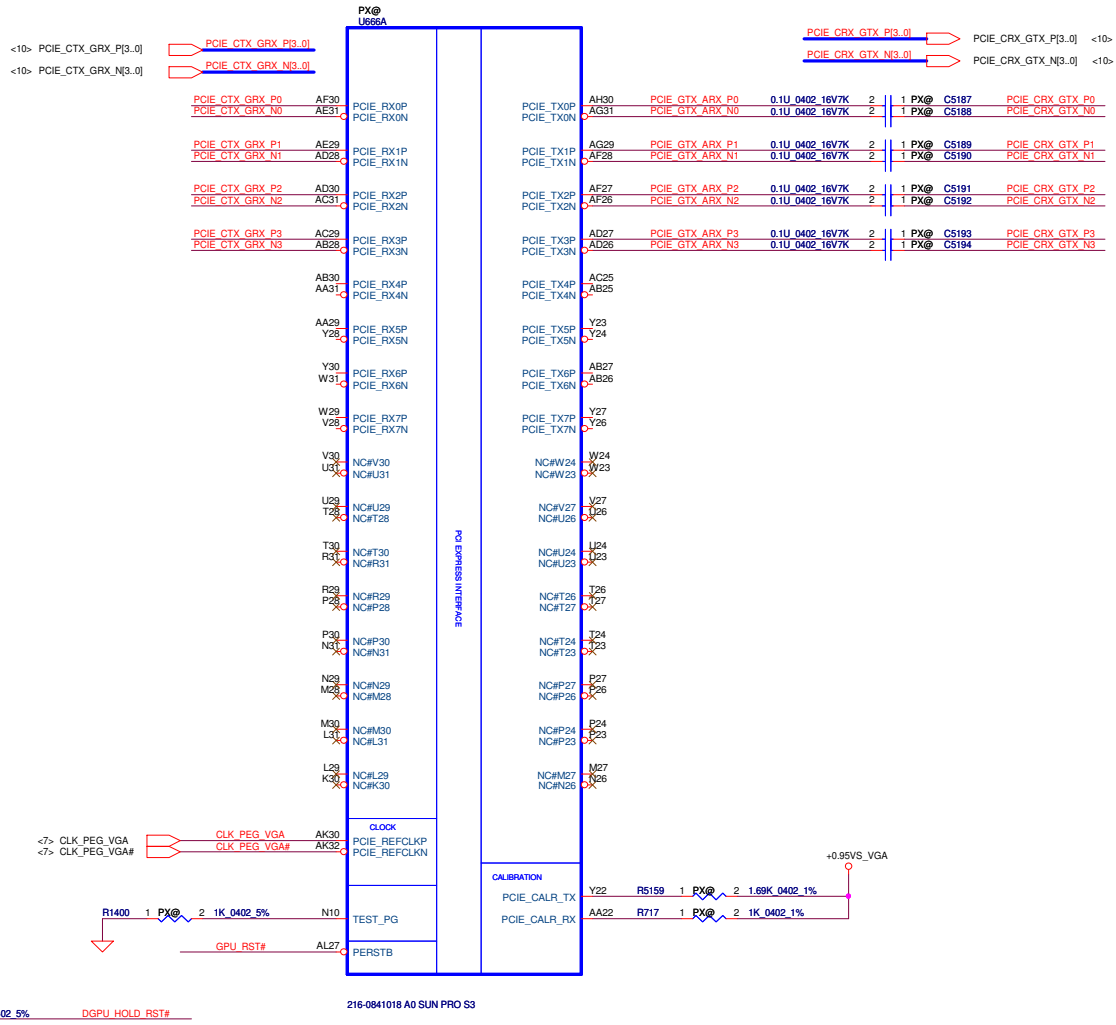
PN:SP07000LT00



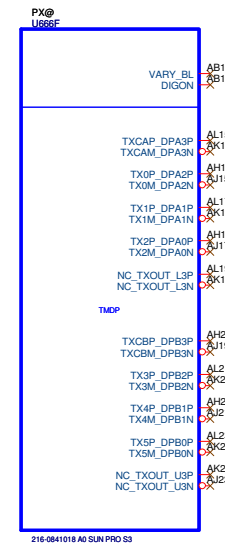
CRB1.0 0.1uF *1 / 2.2uF *1
2.2uF (reserved)



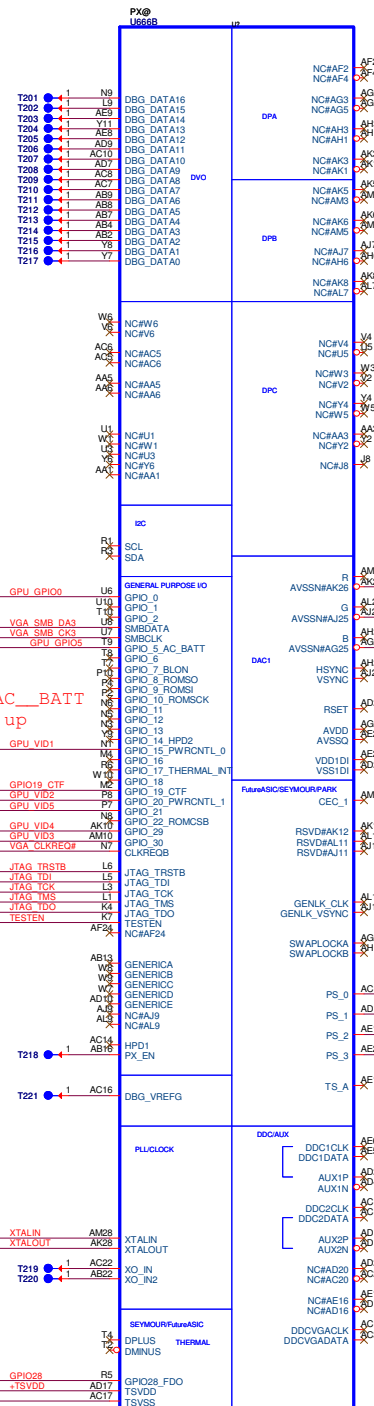
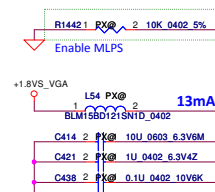
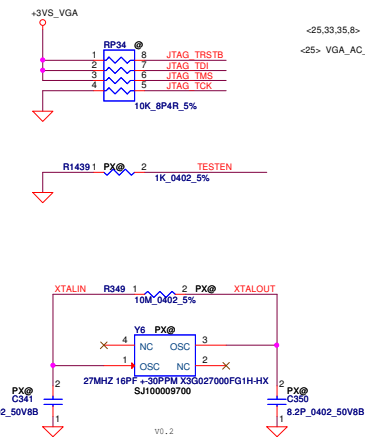
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		DDR/III DIMMA	
2011/12/13		2012/12/13		Document Number	
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Date:		Thursday, March 14, 2013		Sheet 15 of 46	



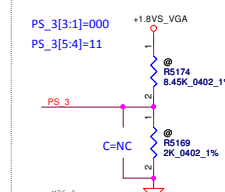
No Use GPU Display Port output



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Date: Thursday, March 14, 2013				Sheet 16	of 46








Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

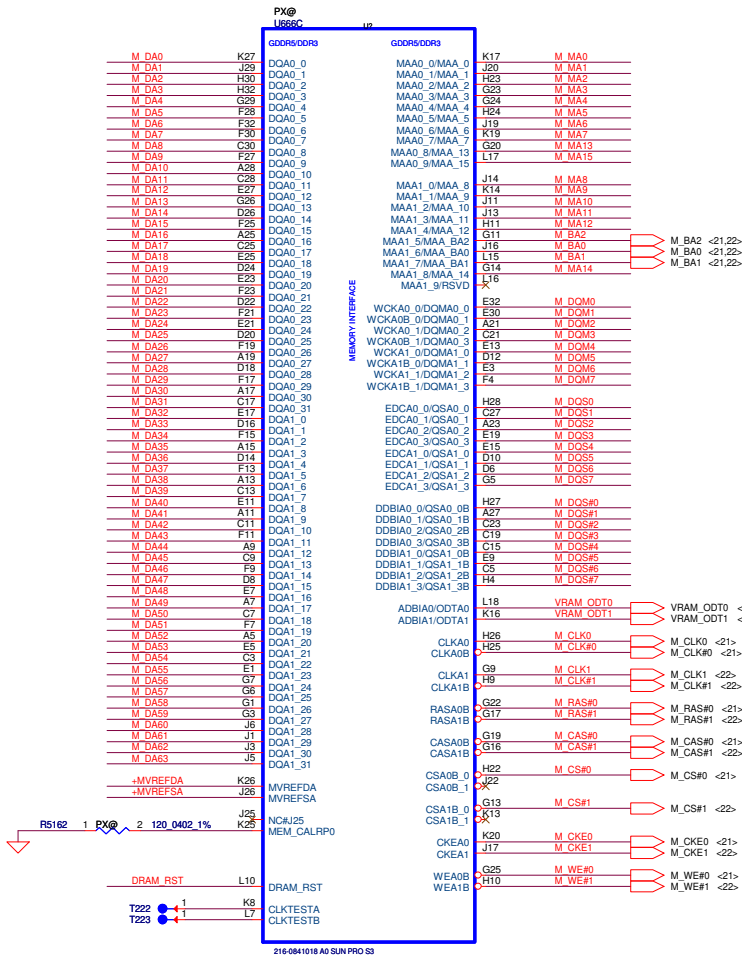
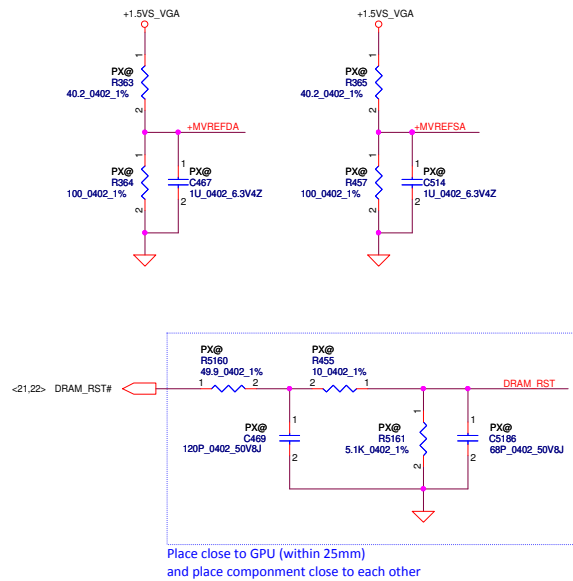


Strap Name :

```
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
```

Memory ID	Memory Type	Configuration	Size
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB
011	SA000068R10	Samsung K4W4G1646B-HC11	2GB
100	SA000065D20	Micron MT41K256M16HA-107G:E	2GB

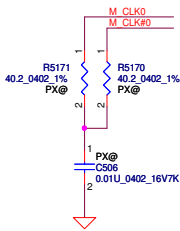
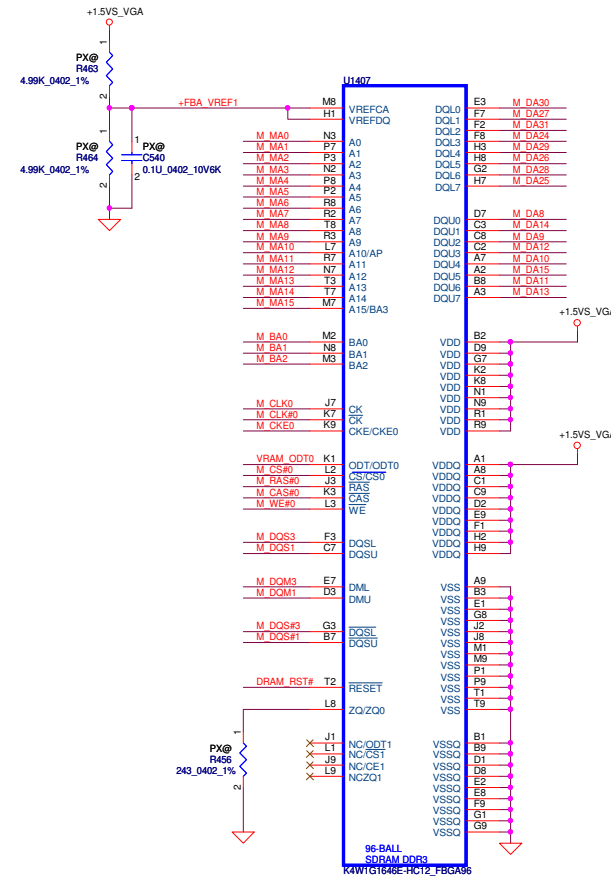
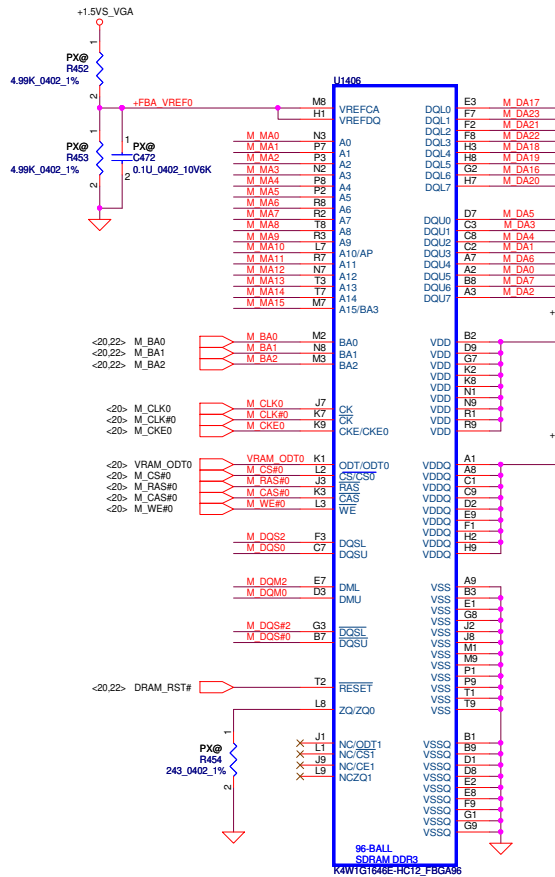
<21,22> M_DA[63..0]  M_DA[63..0]
 <21,22> M_MA[15..0]  M_MA[15..0]
 <21,22> M_DM[7..0]  M_DM[7..0]
 <21,22> M_DQS[7..0]  M_DQS[7..0]
 <21,22> M_DQS# [7..0]  M_DQS# [7..0]



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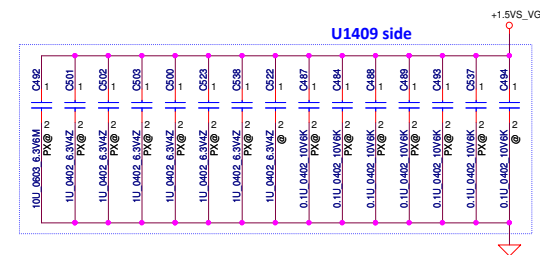
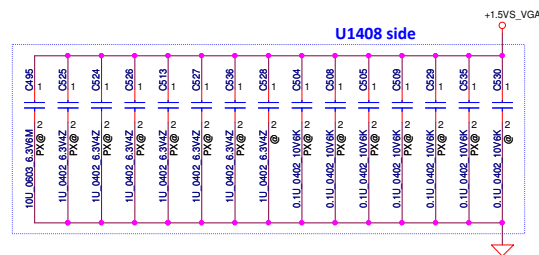
Memory Partition A - Lower 32 bits

- <20,22> M_DA[63..0] M_DA[63..0]
- <20,22> M_MA[15..0] M_MA[15..0]
- <20,22> M_DQM[7..0] M_DQM[7..0]
- <20,22> M_DQS[7..0] M_DQS[7..0]
- <20,22> M_DQS# [7..0] M_DQS# [7..0]

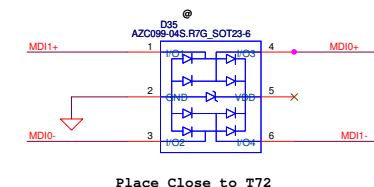
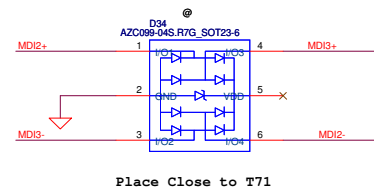
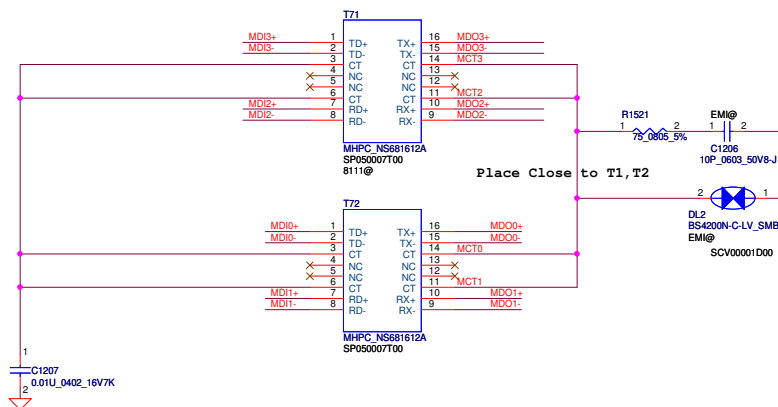
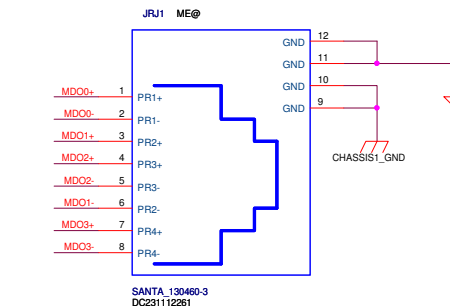
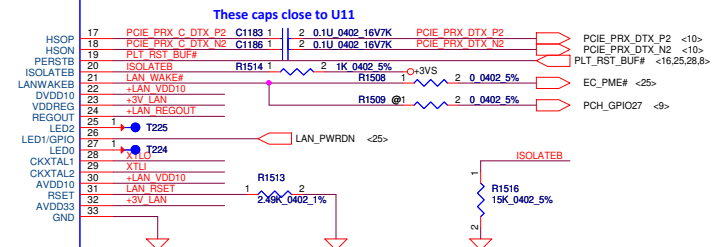
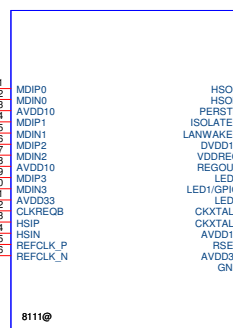
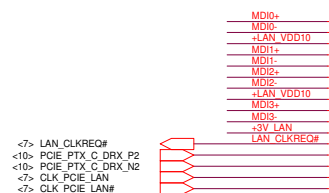
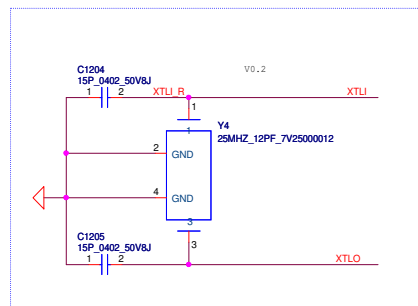
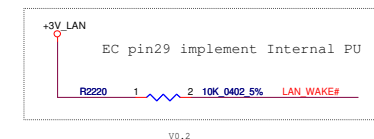
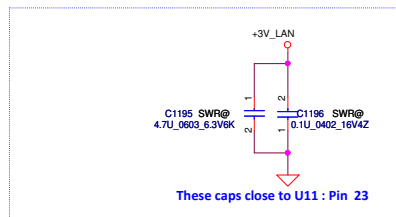


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D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

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Connector: 0.3A / pin

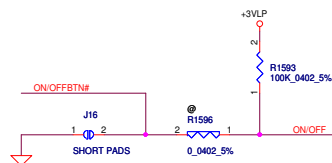
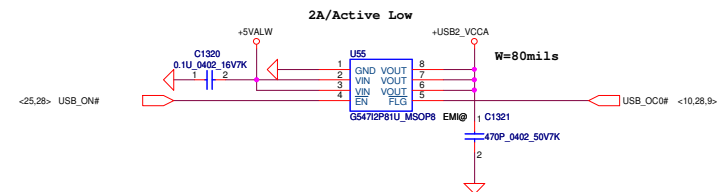


Diagram illustrating the Pin 1 connection for the ACES_51524-0060N-001 SP010014M10. The diagram shows a 6-pin connector with pins 1 through 6. Pin 1 is connected to GND. Pin 2 is connected to BATT_CHG_LED#. Pin 3 is connected to BATT_LOW_LED#. Pin 4 is connected to PWR_LED#. Pin 5 is connected to BATT_LOW_LED#. Pin 6 is connected to +5VALW. A note indicates that pins 5 and 6 are not used (X).



EMI

The diagram illustrates the EMI (Electromagnetic Interference) components for various USB20 signals. It shows the connection between the USB20_P0, USB20_N0, USB20_P2, USB20_N2, USB20_P3, and USB20_N3 signals and the EMI@ components. The signals are connected to the EMI@ components via L50 and L52 components. The EMI@ components are labeled with their respective values: R173, R174, R175, R176, R177, and R178. The values are 0.0402_5% for R173, R174, R175, and R176, and 0.0402_5% for R177 and R178.

WCM-2012-900T_4P

USB20_P0 3 4 USB20_P0 R

SM070000K00

USB20_N0 2 1 USB20_N0 R

L50 EMI@

WCM-2012-900T_4P

USB20_P2 3 4 USB20_P2 R

SM070000K00

USB20_N2 2 1 USB20_N2 R

L51 EMI@

WCM-2012-900T_4P

USB20_P3 3 4 USB20_P3 R

SM070000K00

USB20_N3 2 1 USB20_N3 R

L52 EMI@

USB20_P0 1 2 USB20_P0 R

R173 0.0402_5%

USB20_N0 1 2 USB20_N0 R

R174 0.0402_5%

USB20_P2 1 2 USB20_P2 R

R175 0.0402_5%

USB20_N2 1 2 USB20_N2 R

R176 0.0402_5%

USB20_P3 1 2 USB20_P3 R

R177 0.0402_5%

USB20_N3 1 2 USB20_N3 R

R178 0.0402_5%

IO Board

W=40mils

W=80mils

USB2_VCCA

+3VS

+3VS USB2_VCCA

DMIC_CLK

DMIC_DATA

PLUG_IN#

HP_OUTL

HP_OUTR

EXT_MIC_SLEEVE

EXT_MIC_RING2

MIC2_VREF0

R1594 1 2 2.2K 0402 5%

R1595 1 2 2.2K 0402 5%

C1366 1 10 0.1u 0402

C1307 1 10 0.1u 0402

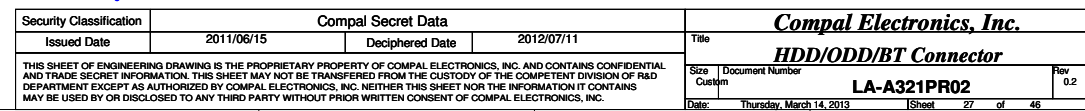
JCR1 ME@

ACES 86514-02401-07

SP010015W00

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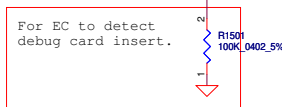
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Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON



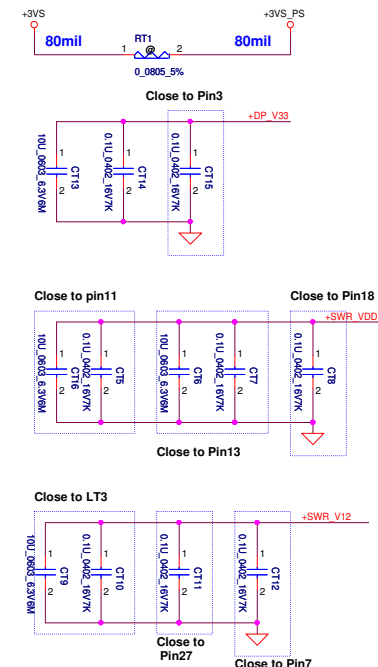
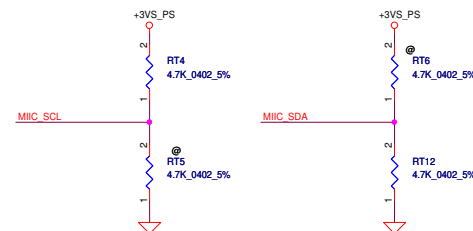
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[illegible]

MIIC_SDA MIIC_SCL	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

EDID_DATA RT9 1 2 4.7K 0402 5%

EDID_CLK RT10 1 2 4.7K 0402 5%



W=60mils

3VS

U46

5 VIN

4 SS

1 2

1500P_0402_50V7K

C614

1 2

4.7U_0603_6.3V6K

C613

1 2

APL3512ABITRG_S0T23-5

1 L

2

100K_0402_5%

R939

1 2

0.4042_5%

R1471

1 2

0.4042_5%

R1470

1 2

0.4042_5%

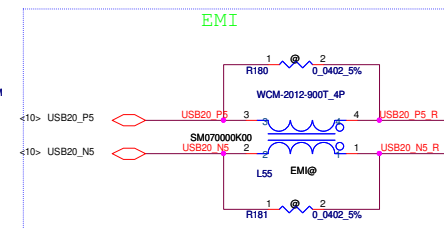
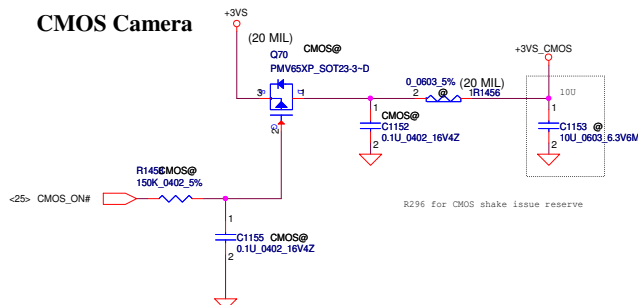
TL_ENVDD

PCH_ENVDD

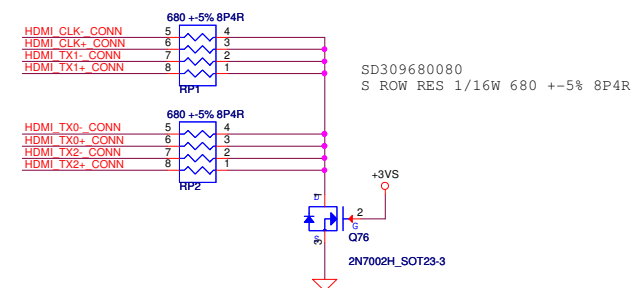
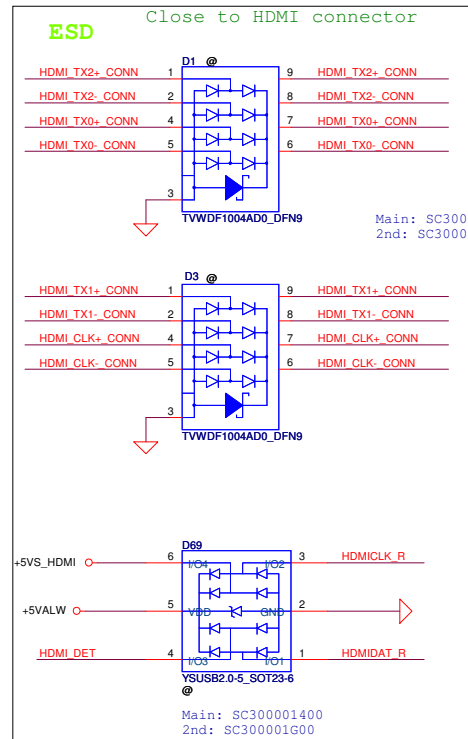
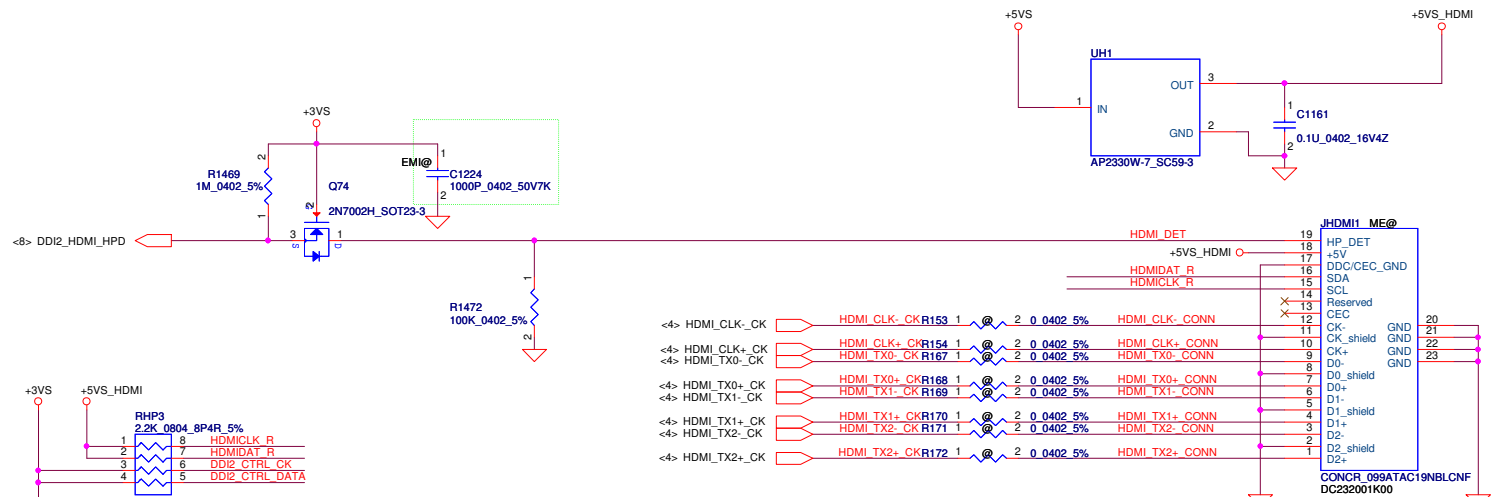
<8>

W=60mils

CMOS Camera



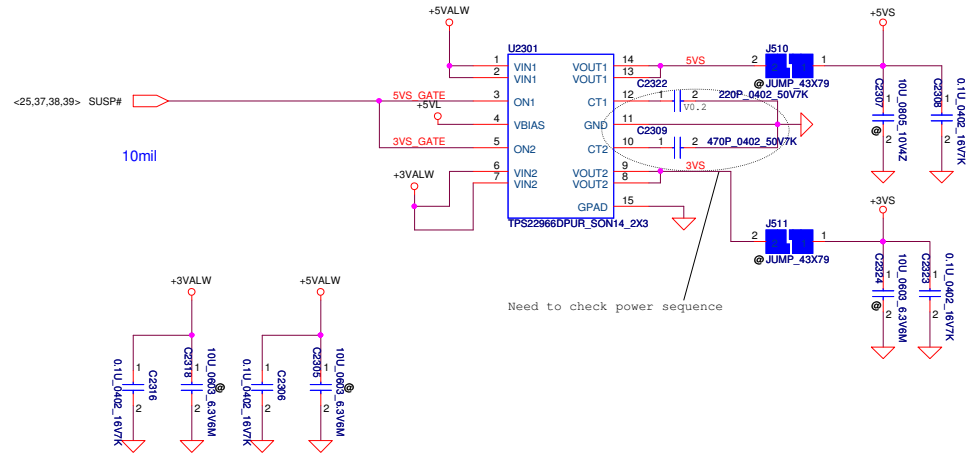
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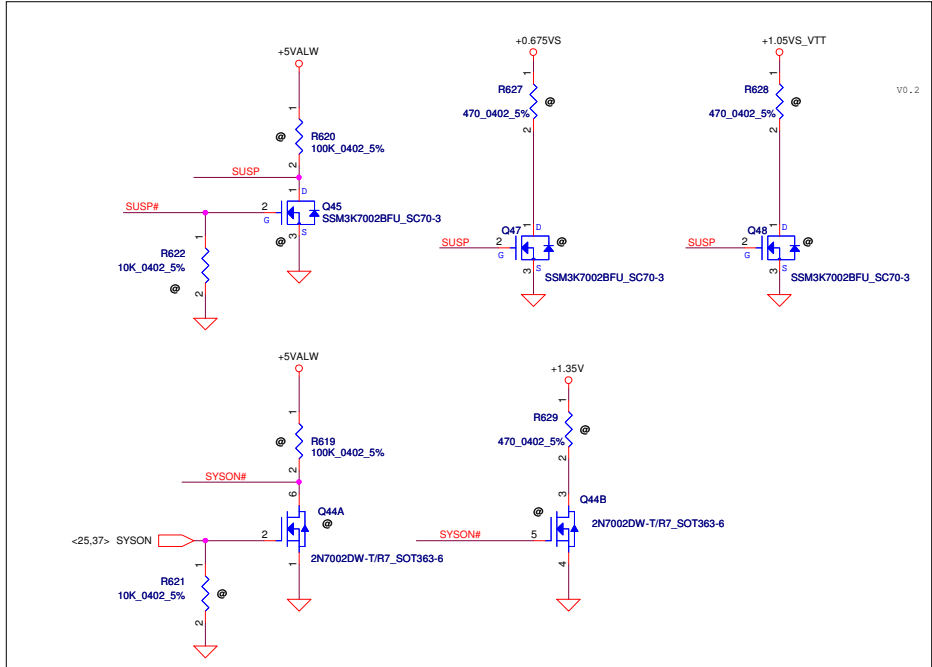
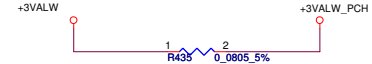
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	HDMI CONN
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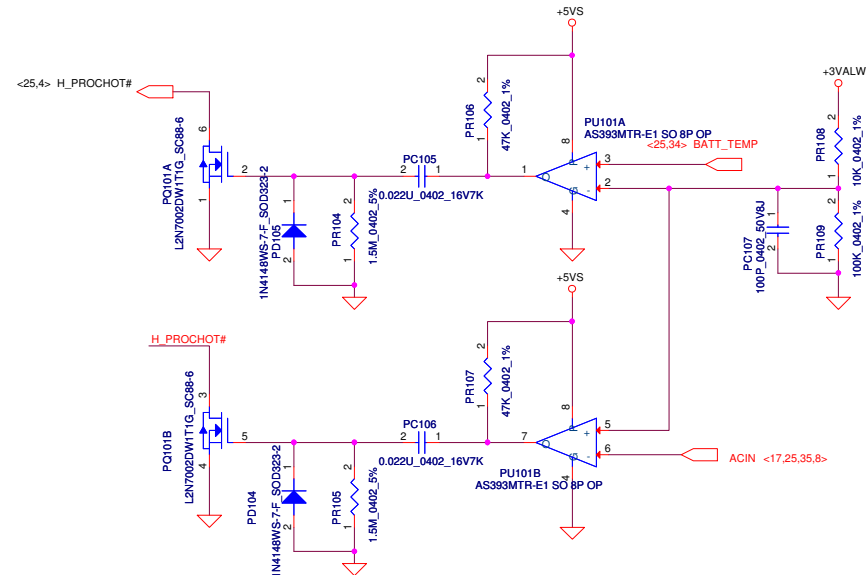
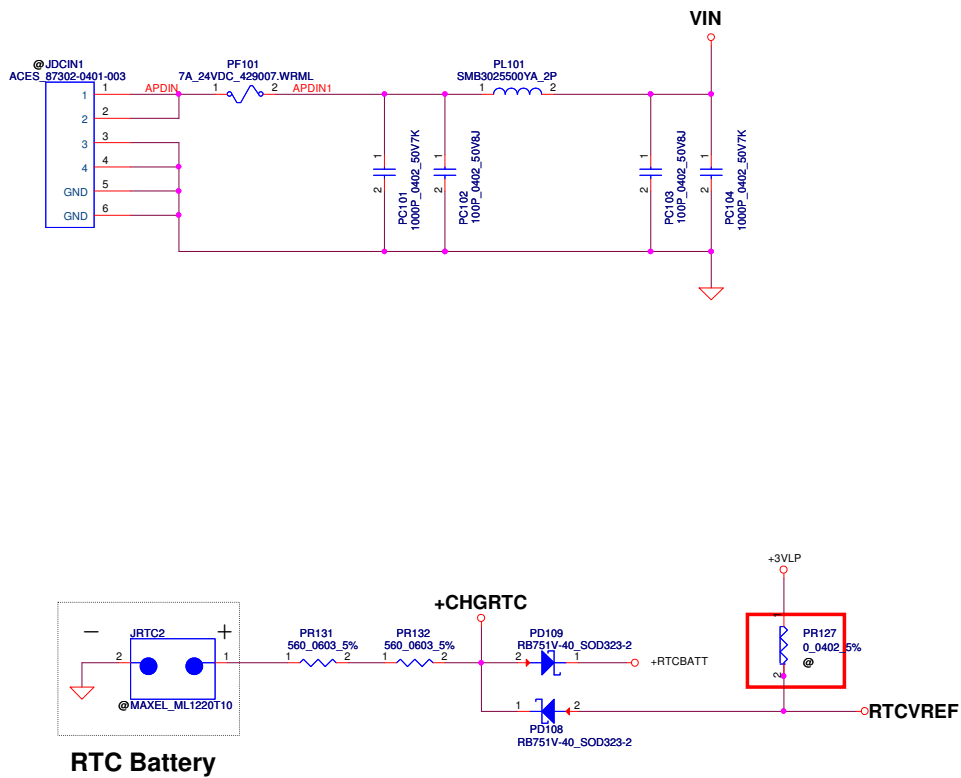
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)



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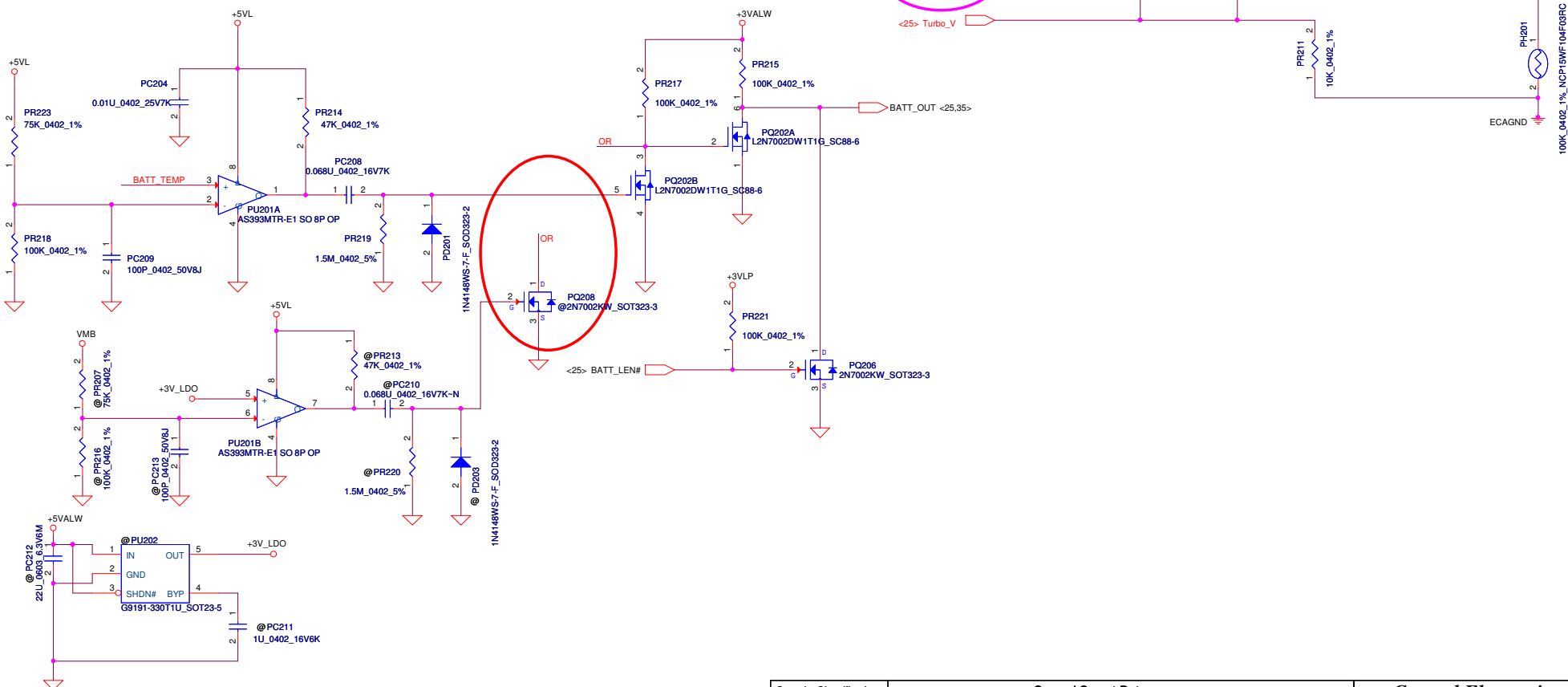
PWR DCIN

Document Number
LA-A321PR01

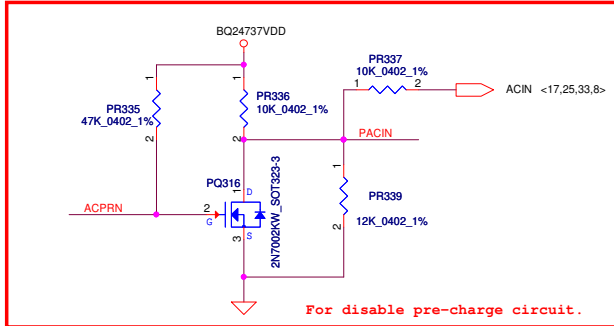
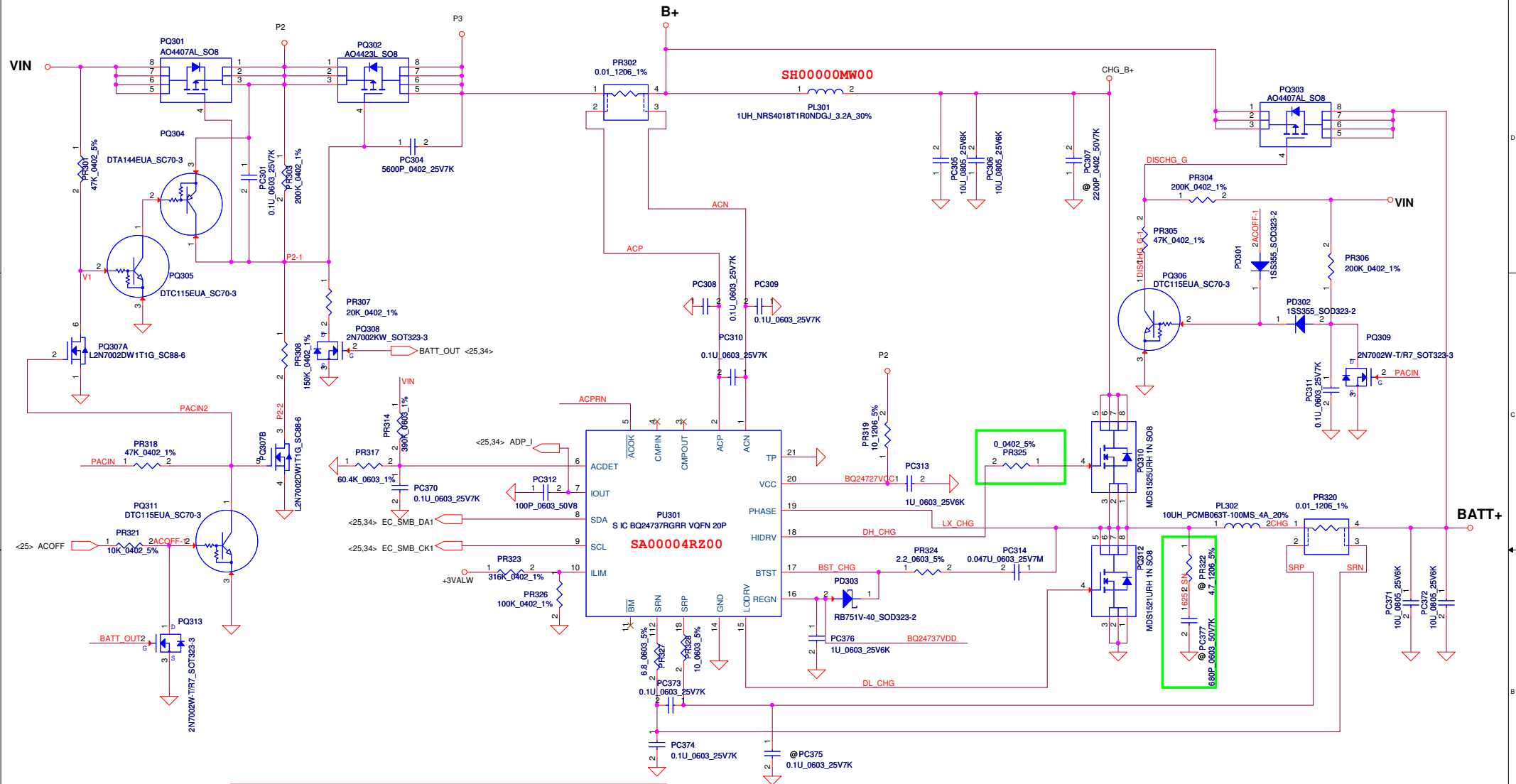
Date: Thursday, March 14, 2013

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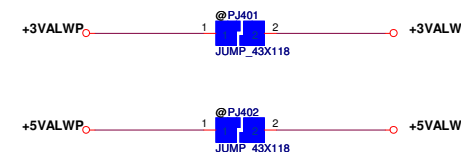
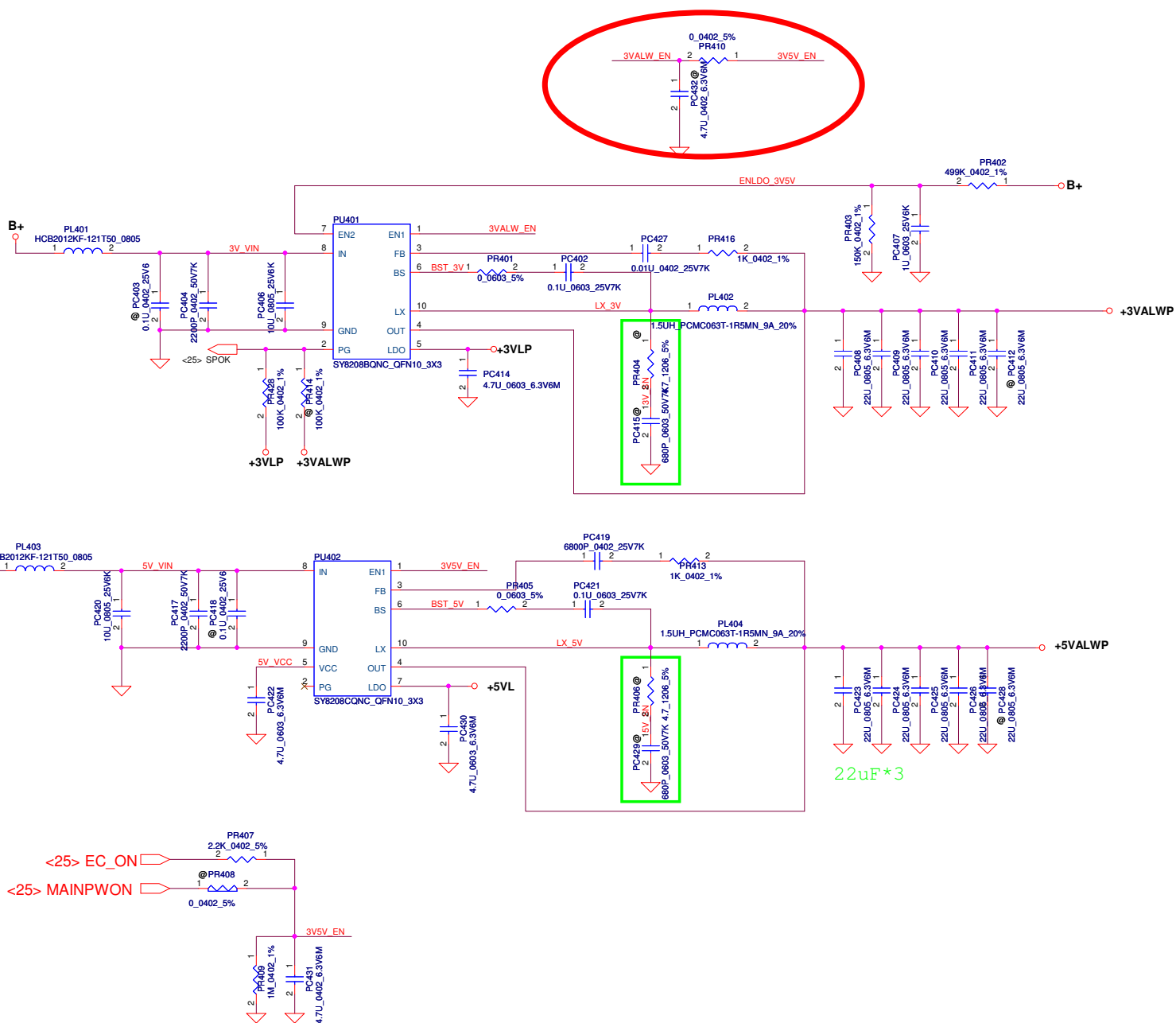
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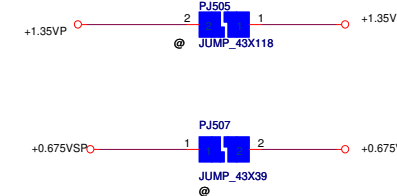
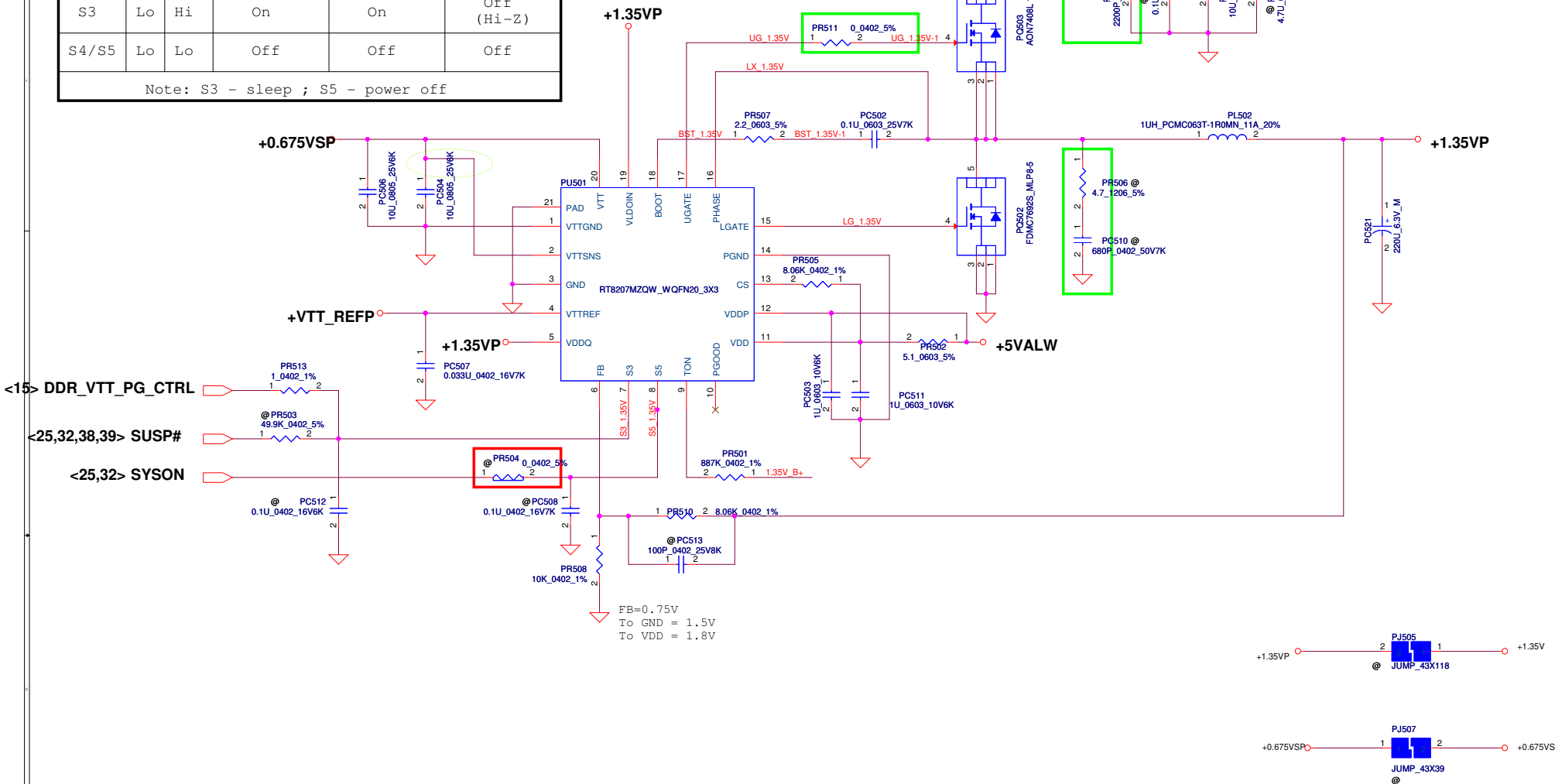
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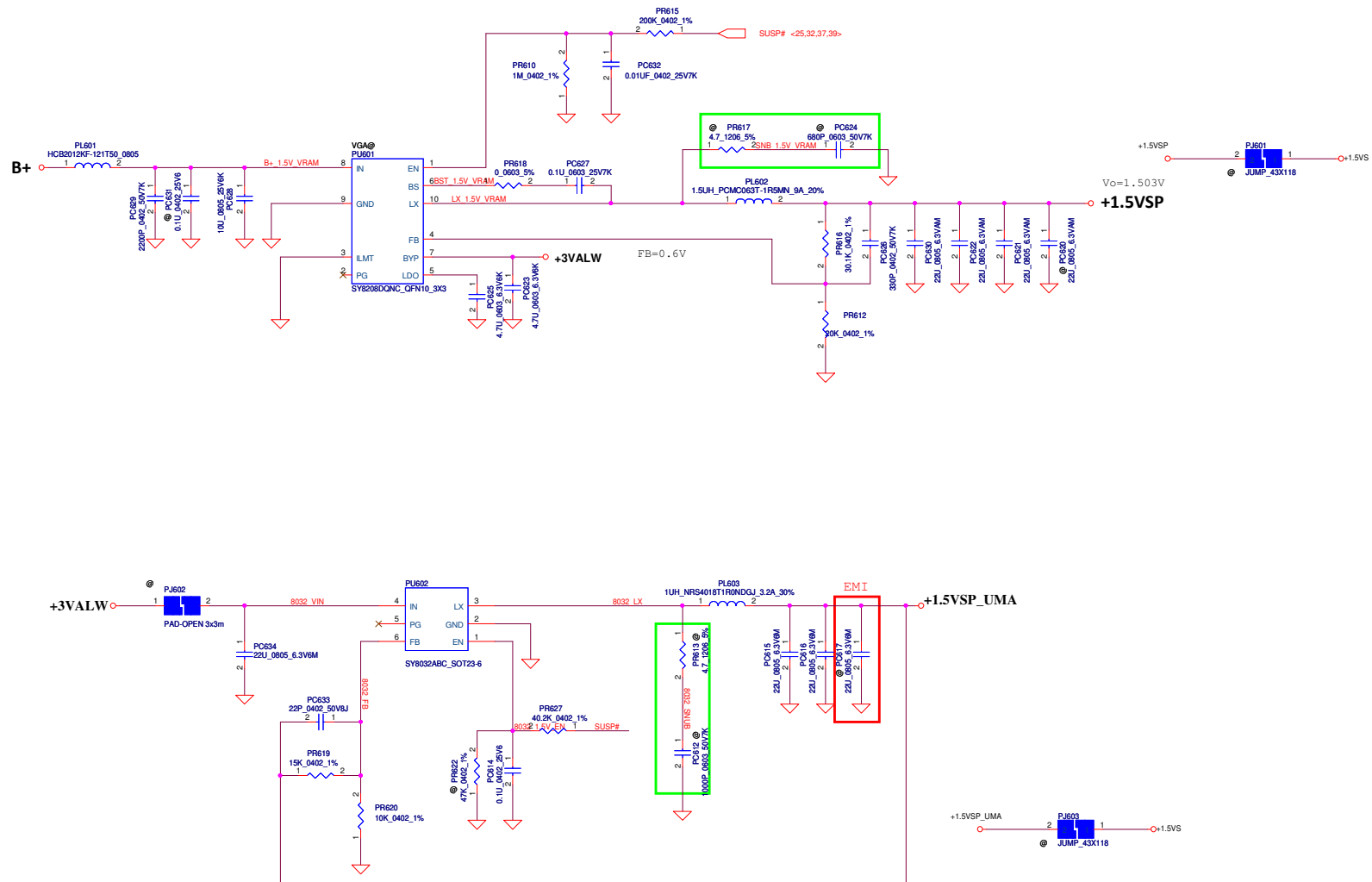
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

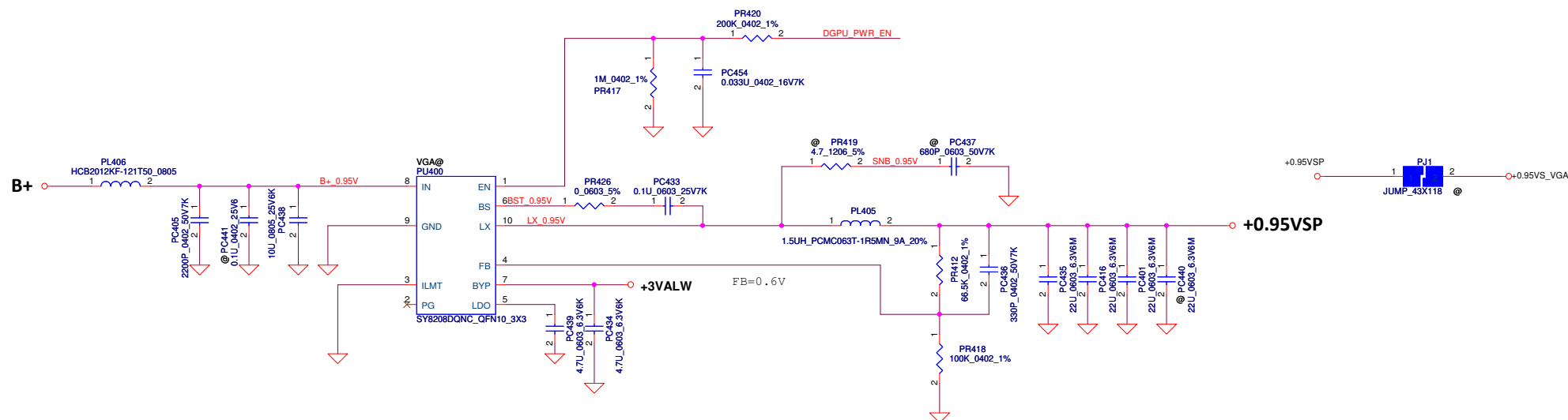
Note: S3 - sleep ; S5 - power off



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1.8V controller (35.15), Support component (35.16)



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+CPU_CORE

30 X 22u/0805

RF request

Reserve

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Item	Modify List	PG#	Reason for change	Date	Phase
1	For HW sequence	44	ADD PR821 100K ohm pull high +VS_VGA	3/11	SDV
2	For HW sequence	37	Remove PC512 0.1U_0402	3/11	SDV
3	For HW sequence	39	Change PC443 to 0.1U_0402	3/11	SDV
4	For HW sequence	40	Change PC186 to 0.1uf	2/7	SDV
5	For HW sequence	40	Change PC454 to 0.033uf	2/7	SDV
6	For HW sequence	40	Change PR183 to 47K ohm	2/7	SDV
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size Custom	
Document Number				Rev	
C38-AMD KABINI Schematic				0.2	
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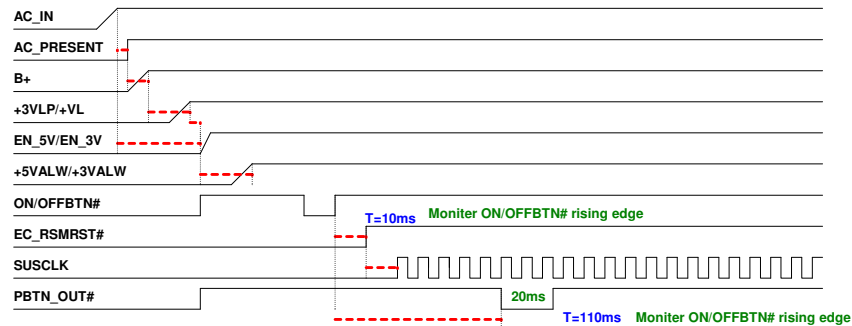
Version change list (P.I.R. List)

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for HW

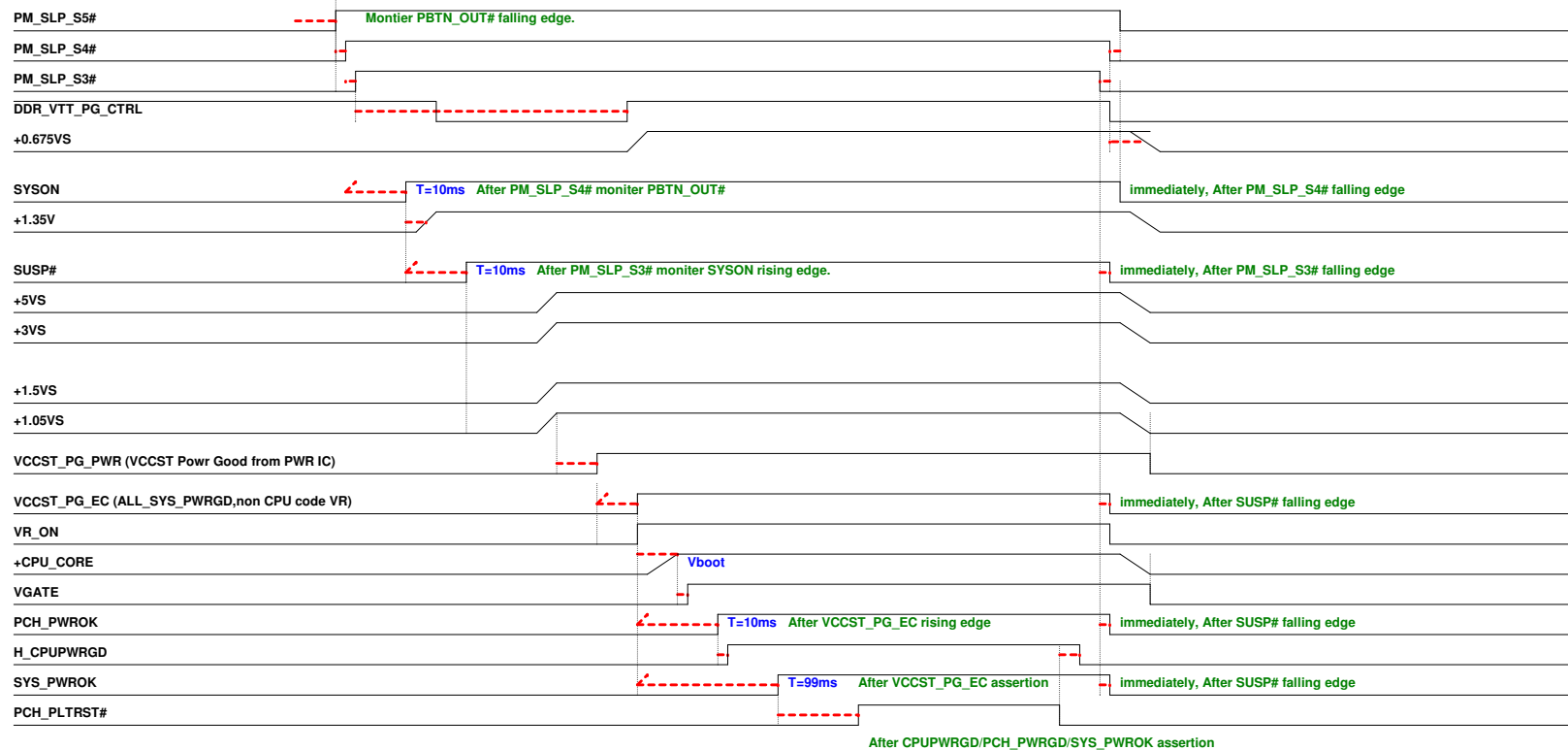
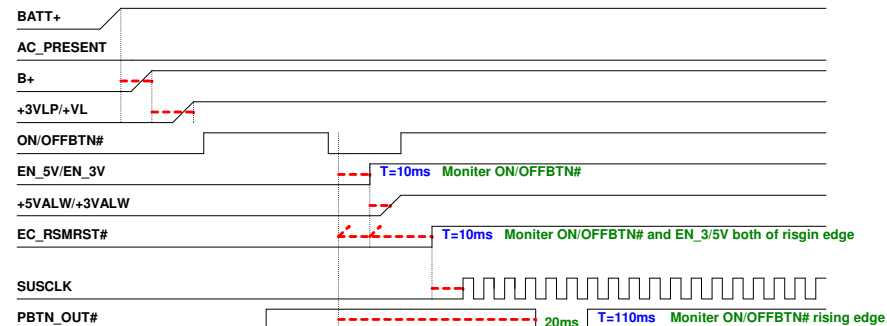
Item	Reason for change	PG#	Modify List	Date	Phase
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2					
3					
4					
5					
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13					
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17					

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